

Usable only for Hpe_IRP2

General Description:

The HC-PCIeX1hs is a high speed child board. This means up to 10 LVDS pairs are connected directly to the FPGA SERDES.

On this child board is a PCI Express X4 over cable connector. There are 2 population options available, depending on the developer's requirement.

-d option: downstream board

Root complex in PC

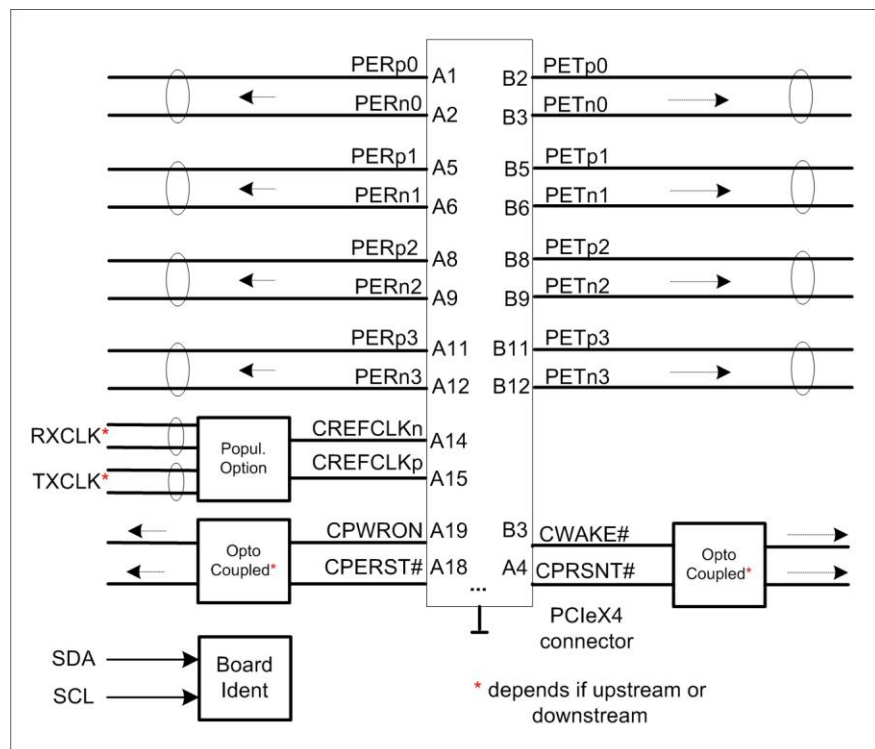
-u option: upstream board

Root complex in Hpe_IRP2



Sorry the population option can be done only during manufacturing.

Block diagram:



Pin description:

A1	GND	A2	GND	B1	X1B_WAKE_TX	B2	X1B_WAKE_RX#
A3	RX_DATA0+	A4	GND	B3	X1B_PWRGD_TX	B4	X1B_PWRGD_RX#
A5	RX_DATA0-	A6	GND	B5	X1B_RESET_TX#	B6	X1B_RESET_RX
A7	GND	A8	GND	B7	X1B_PWRON_TX	B8	X1B_PWRON_RX#
A9	TX_DATA0+	A10	GND	B9	NC	B10	NC
A11	TX_DATA0-	A12	GND	B11	NC	B12	NC
A13	GND	A14	GND	B13	NC	B14	NC
A15	RX_DATA1+	A16	GND	B15	VCC3V3	B16	GND
A17	RX_DATA1-	A18	GND	B17	VCC3V3	B18	GND
A19	GND	A20	GND	B19	VCC3V3	B20	GND
A21	TX_DATA1+	A22	GND	B21	VCC3V3	B22	GND
A23	TX_DATA1-	A24	GND	B23	VCC3V3	B24	GND
A25	GND	A26	GND	B25	VCC3V3	B26	GND
A27	RX_CLK+	A28	GND	B27	VCC3V3	B28	GND
A29	RX_CLK-	A30	GND	B29	VCC3V3	B30	GND
A31	GND	A32	GND	B31	NC	B32	I2C_SCL
A33	GND	A34	GND	B33	NC	B34	GND
A35	TX_CLK+	A36	GND	B35	NC	B36	I2C_SDA
A37	TX_CLK-	A38	GND	B37	V12V0 - NC	B38	GND
A39	GND	A40	GND	B39	V12V0 - NC	B40	GND
A41	GND	A42	GND	B41	V12V0 - NC	B42	GND
A43	RX_DATA2+	A44	GND	B43	V12V0 - NC	B44	GND
A45	RX_DATA2-	A46	GND	B45	V12V0 - NC	B46	GND
A47	GND	A48	GND	B47	V12V0 - NC	B48	GND
A49	TX_DATA2+	A50	GND	B49	V12V0 - NC	B50	GND
A51	TX_DATA2-	A52	GND	B51	V12V0 - NC	B52	GND
A53	GND	A54	GND	B53	NC	B54	NC
A55	RX_DATA3+	A56	GND	B55	X1B_BOARD_TP1	B56	X1B_BOARD_TP7
A57	RX_DATA3-	A58	GND	B57	X1B_BOARD_TP2	B58	X1B_BOARD_TP8
A59	GND	A60	GND	B59	X1B_BOARD_TP3	B60	NC
A61	TX_DATA3+	A62	GND	B61	X1B_BOARD_TP4	B62	NC
A63	TX_DATA3-	A64	GND	B63	X1B_BOARD_TP5	B64	NC
A65	GND	A66	GND	B65	X1B_BOARD_TP6	B66	NC

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