

The graphic features the Hpe JTAG logo with a chameleon and a percentage sign, the text 'adaptive & affordable Boundary Scan Solutions', and the 'python powered' logo. A hand holds a USB-Dongle connected to a PCB. A stack of software upgrade blocks is shown: 'Python Scriptable', 'Python Macros Enabled', 'INTEST/EXTEST', and 'SAMPLE 0 - Euro'. A blue arrow labeled 'Easy Upgrade' points from the stack to the USB-Dongle. A white Hpe JTAG dongle is connected to the PCB via a cable.

Hpe[®] JTAG
adaptive & affordable
Boundary Scan Solutions

... for interactive or
automated PCB & IC debugging

python
powered

USB-Dongle

Python Scriptable

Python Macros Enabled

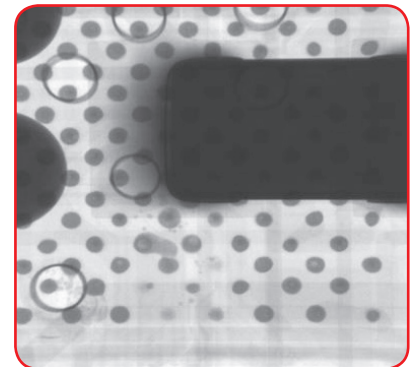
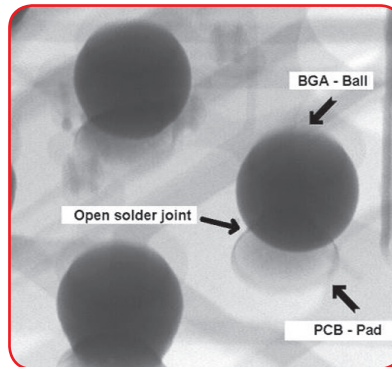
INTEST/EXTEST

SAMPLE 0 - Euro

Easy Upgrade

- **Adaptive & affordable Boundary Scan**
For interactive or automated PCB and IC debugging
- **Free basic software, easy upgrades**
Download free basic software, supporting sample mode, from www.hpe-jtag.com. Install upgrades as needed.
- **Signal-Filtering**
Observe only signals of interest
- **BSDL- and Pin-File Parser**
Import BSDL or HDL top-level port names to find signals quickly
- **Scripting interface**
For automation and extensions, even custom specific GUIs

Today's electronic systems contain more and more BGAs (ball grid arrays). Very often signals are no longer accessible on the PCB, so that faults like shorts or opens can only be found with expensive x-ray equipment or boundary scan solutions. The x-ray pictures show two of the most common problems designers might run into when using BGAs: shorts and open solder joints.



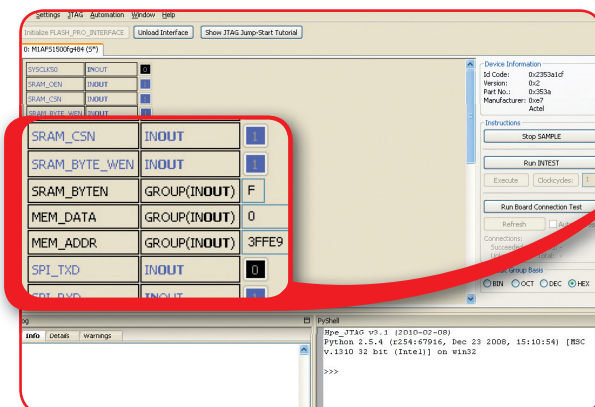
Hpe®_JTAG enables designers to debug their PCBs interactively (without the need to program a design into the PLDs), observe and debug their PLD designs, write scripts for all repetitive tasks and even setup automated tests, e.g. for limited lot productions.



Hpe®_JTAG supports the following JTAG instructions:

- **SAMPLE:** The SAMPLE instruction is used to get a snapshot of the current pin states of a device in the JTAG chain. It does not influence the device operation.
- **EXTEST:** The EXTEST instruction is used to check a connection between devices in one JTAG chain. The values of output pins can be set and the values of input pins can be read. In combination with the scripting interface EXTEST can be used to generate any testpattern. Examples for flash programming, SPI, I2C protocols etc. are preinstalled.
- **INTEST:** If supported by the device, the INTEST instruction is used to check the internal functionality of a device in the JTAG chain. The values of input pins can be set and the values of output pins can be read.

Hpe®_JTAG provides a graphical user interface, but also powerful Python-scripting capabilities. Instead of graphically representing huge ball grid arrays with more than thousand IOs each, devices are represented by tabs. A filter function allows the user to display only signals that are currently of interest. The screenshot below shows an example for a scan chain containing just a single device.



IO-Filtering

Observe only IOs of interest

Import signal names

from BSDL-files or PLD vendor pin-files (port names of your HDL top-level entity)

Bus grouping

Observe individual signals or group signals as buses

Visit www.hpe-jtag.com for free software!



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