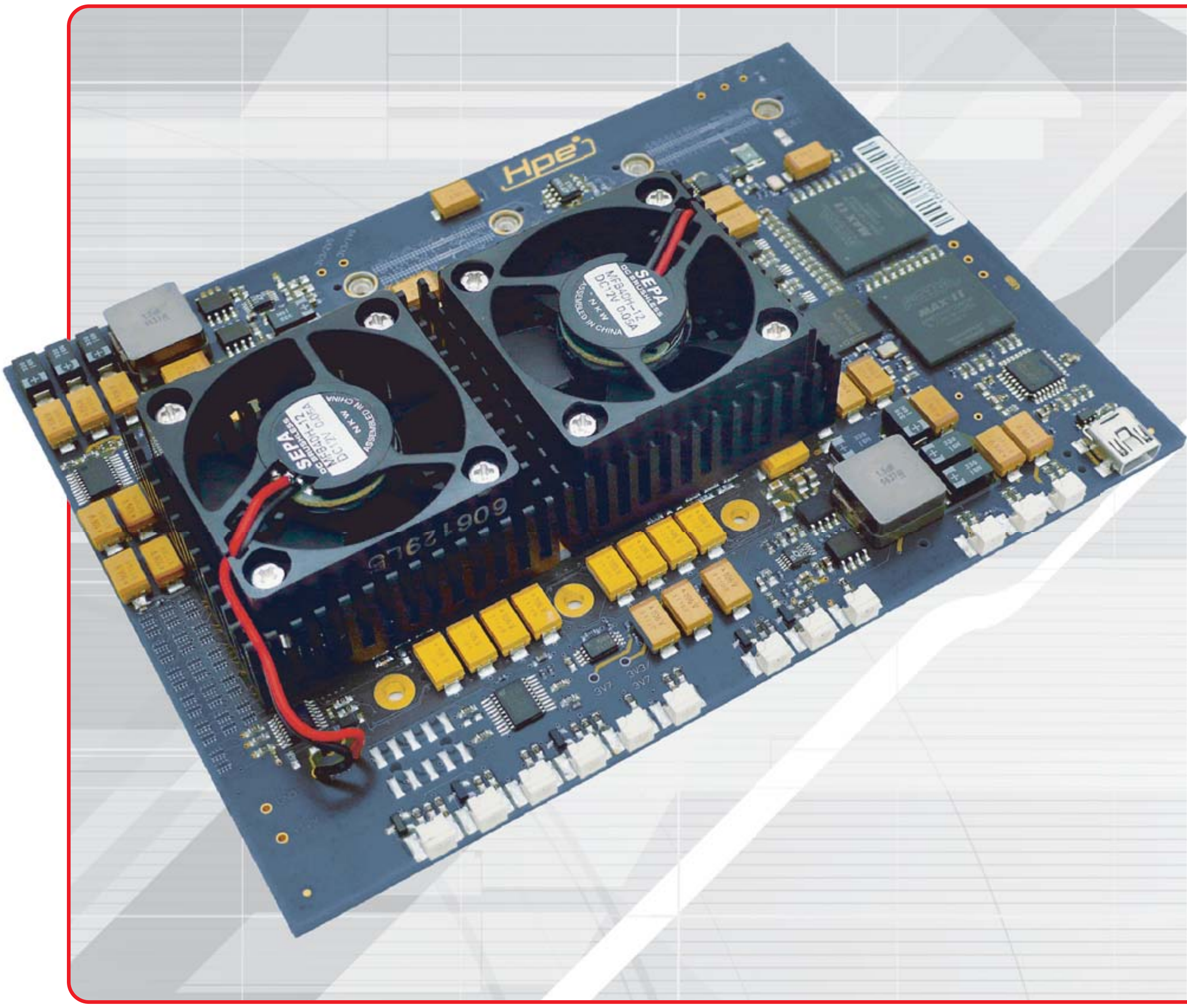
Gleichmann Electronics Research



Hpe® midi

User Manual for HMX2-AS2

HMX2-AS2 manual

Martina Zeinzinger
Version: 2010-03-17

Copyright Notice

Contents

1 Introduction

Attention
The *HMX2-AS2* is a FPGA development system therefore it is not designed for a worst case scenario. If it is used with very high performance, it is possible that the FGPAs are not cooled sufficiently and/or the case overheats. It is the user's responsibility to proof the feasibility of the FPGA-design. If this protection mechanism is evaded, the consequence is the expiration of any guarantee.

The name *HMX2-AS2* stands for *Hpe Module X2 stuffed with Altera Stratix II FPGAs*. *HMX2-AS2-180* means that the FPGAs *EP2S180F1508C3N* are stuffed.

The *HMX2-AS2* is designed to be used in conjunction with the mainboard *Hpe_midi*. The module is compatible to the former FPGA modules from *Gleichmann Electronics Research*, however, the mechanical outlines are different. Two *Altera Stratix II* devices are the main part of this module which can be used for the functional verification of high complex digital circuits and for *SEmulation*. The connection to the mainboard is done by two elastomer module connectors.

1.1 System Overview

The following features are the most important parts of this FPGA module:

- two 1508 pin *Altera Stratix II* FPGAs *EP2S180F1508C3N* (*DUT-FPGA#1* and *DUT-FPGA#2*)
- two 364 pin elastomer module connectors (X1, X2)
- two 132 pin elastomer *Hpe_childboard* connectors (X3, X4), one with low voltage differential signals (LVDS)
- flash for the configuration of the FPGAs
- CPLD for clock distribution (clock factory), configuration and fan control
- CPLD for FPGA Code Protection (FCP) and *Altera USB Blaster*

The FPGAs on the *HMX2-AS2* are the biggest and the fastest ones of their family and they are used in a 1508-pin package.

The naming convention of this manual is based on the assumption that the *HMX2-AS2* is used together with the *Hpe_midi* and the *Hpe_childboard HC-PCIe* in the *SEmulator* mode. The *HC-PCIe* has to be stucked on the *Hpe_childboard* connector X3 and mainly consits of of an FPGA—the *Communication Controller*—which handles the connection to the PC via *PCI Express*. Figure 1.1 gives you a graphical overview of the components on the *HMX2-AS2*.

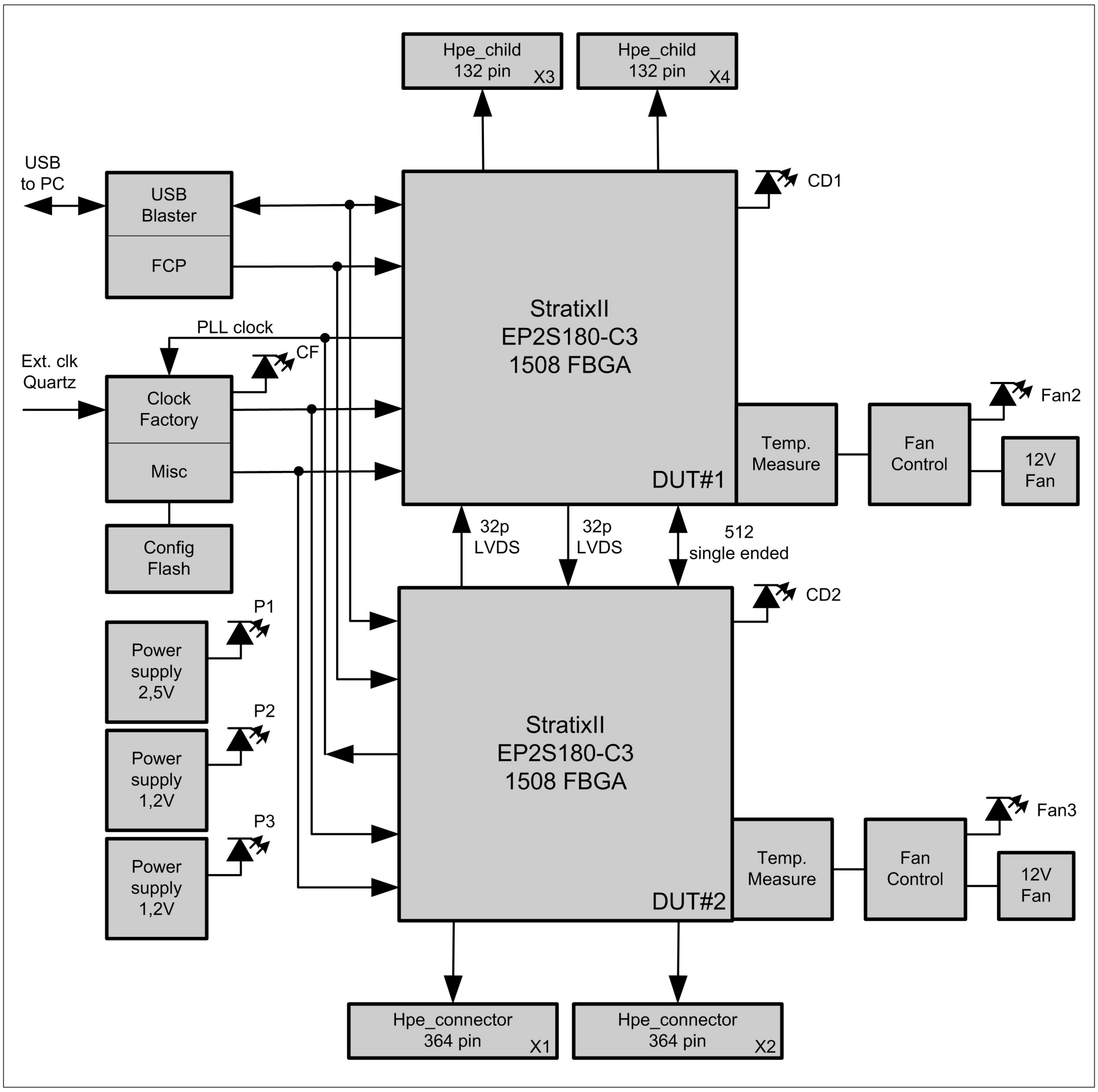


Figure 1.1: The *HMX2-AS2* Block Diagram

2 General Information

2.1 Reset

There is one system wide reset (*PWR_RESET#*) which resets all CPLDs and FPGAs on the *HMX2-AS2*. The reset is low active, activated after power up and controlled by a supervisor on the *Hpe_midi*.

2.2 LEDs

Looking at the front side of your *HMX2-AS2* you find twelve LEDs. If the *HMX2-AS2* is in the case together with a mainboard, you find the LEDs on the front side in the upper row (refer to figure 2.1).

The first three LEDs from the right side are yellow and in a box named *Fan*. The right LED shows the activity of of the fan for the *Communication Controller* on the *HC-PCIe*. The LED in the middle shows the fan activity for the *DUT-FPGA#1* and the left one shows the fan activity for the *DUT-FPGA#2*.

The next three LEDs are green and in a box named *Power*. The right one shows power good for 2.5 V and the one in the middle signals signals power good for the 1.2 V core voltage of the *DUT-FPGA#1* and the left one signals power good for the 1.2 V core voltage of the *DUT-FPGA#2*.

The next three LEDs are in a box named *ComCon*. Two are blue and one is yellow. These LEDs can only be lit when the *HC-PCIe* is connected. The right one (yellow) stands for *data transfer* (DT), the one in the middle signals *JTAG connection to the PC via PCI Express* (PC) and the left one shows that the connection between the *Communication Controller* and the DUTs is ready (CC).

The three blue LEDs on the left side are named *Config Done*. The right one shows that the *Clock Factory* (CF) is prepared, the one in the middle signals that the *DUT-FPGA#1* is configured and the left one signals that the *DUT-FPGA#2* is configured.

2.3 AES

AES is a block cipher standard. *DUT-FPGA#1* and *DUT-FPGA#2* can be protected with AES. The key for AES can only be programmed once to each FPGA. That is to say, when the key is programmed, it can be neither changed nor deleted any more. Each configuration for this protected FPGA has to be encrypted with the key before it is configured to the FPGA. In the FPGA the bit stream is decrypted with the same key during configuration.

If you wish to use the AES, please contact *Gleichmann Electronics Research*, because the generation and programming of the key has to be done in our factory.

Due to the fact that with this methode, it is not possible to use the FPGA without encryption any more, there is an alternative technology realised on the *HMX2-AS2*: The FCP. For more information refer to section 4.1.

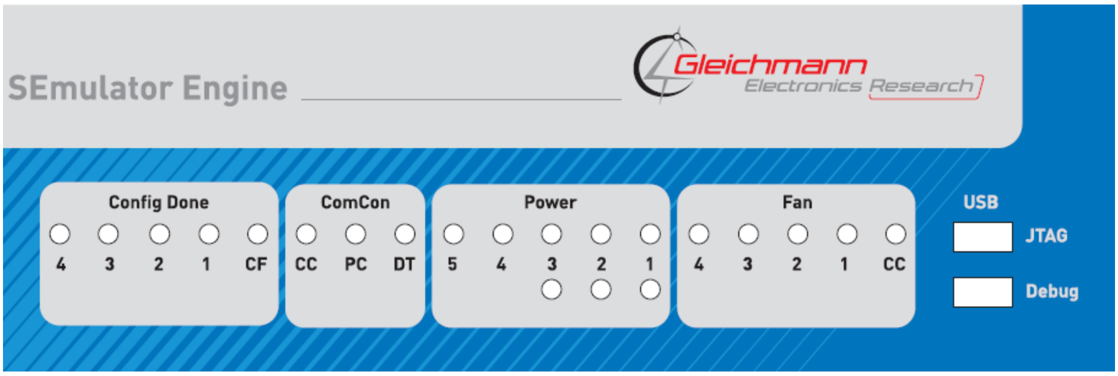


Figure 2.1: The front side of the *SEmulator* Engine

3 Clock Factory

3.1 Clock Distribution

The mainboard delivers three clocks (two from a socket and one from external) to the *CPLD for Clock Factory and Configuration*. Moreover, one PLL output from the *DUT-FPGA#1* and seven PLL outputs from the *DUT-FPGA#2* are connected to the *CPLD for Clock Factory and Configuration*. The clocks can be distributed to most of the clock pins of both DUTs (refer to figure 3.1). The rules how the clocks are distributed are made by the user. He/She is provided a GUI with the *Hpe_desk*, where the connection can be determined. After this step the *CPLD for Clock Factory and Configuration* has to be reconfigured.

A red line in the figure indicates a differential signal pair. For more information how the *CPLD for Clock Factory and Configuration* is connected to the *DUT-FPGA#1* refer to section 7.3 respectively 8.3. In section 7.3.2/8.3.2 you find the clock input pins which are connected from the *CPLD for Clock Factory and Configuration* to the *DUT-FPGA#1*/*DUT-FPGA#2* and in section 7.3.5/8.3.4 pins for the clock output connection from the *DUT-FPGA#1*/*DUT-FPGA#2* to the *CPLD for Clock Factory and Configuration* can be seen. Concerning the clock output from the *DUT-FPGA#1*/*DUT-FPGA#2*: Although the *CPLD for Clock Factory and Configuration* can not handle differential clocks, it is possible to use both signals (the positive and the negative one) as independent single ended connection.

Because it is possible for the user to determine the clock distribution, it is necessary that the *CPLD for Clock Factory and Configuration* is reconfigured each time this distribution has changed. This is done by the *Hpe_desk* via the JTAG chain (*Altera USB Blaster*) or via the *Communication Controller* on the *HC-PCIe*.

In table 3.1 you can find the clocks that have equal lengths to both DUTs.

Pin on DUT1	*Pin on DUT2*
DUT1_CLK3P	DUT2_CLK3P
DUT1_CLK6P	DUT2_CLK6P
DUT1_CLK7-	DUT2_CLK7-
DUT1_CLK7+	DUT2_CLK7+
DUT1_CLK9P	DUT2_CLK9P
DUT1_CLK12P	DUT2_CLK12P
DUT1_CLK15-	DUT2_CLK15-
DUT1_CLK15+	DUT2_CLK15+

Table 3.1: Clocks that are length matched

3.2 Configuration via Flash

It is possible to configure the *DUT-FPGA#1* and the *DUT-FPGA#2* by the *CPLD for Clock Factory and Configuration*. The configuration data is stored in the flash as **.pof files*. The flash disposes of common flash interface (CFI). The *Altera MAXII* parallel flash loader (PFL) feature in the *CPLD for Clock Factory and Configuration* provides an easy way to program the flash memory device through the JTAG interface, and the logic to control configuration from the flash memory device to the two DUTs. The FPGA is configured immediately after power up.

3.2.1 Flash Loading

For generating the **.pof* file for the flash the some steps have to be taken in the Quartus® software. First choose *File – Convert Programming Files...* and make the following settings:

- *Programming file type: Programmer Object File (.pof)*
- *Configuration devilce: CFI_128MB*
- *Mode: Fast Passive Parallel*
- *File name:* choose a name for the output file in this box
- check *Memory Map File*
- *Options...* set *Start address (32-bit hexadecimal): 0xC00000*
- select *SOF Data* in the *Input files to convert* window
- click to *Add File...* and choose the **.sof* file for the *DUT-FPGA#2*
- click to *Add File...* again and choose the **.sof* file for the *DUT-FPGA#1*
- click to *Generate*

After having generated your **.pof* file, you can open the *Programmer* in the Quartus® software. Provided that the usb cable is connected to the *HMX2-AS2* and to your PC choose *USB Blaster [USB-x]* (*x* stands for a number) with the button *Hardware Setup...*. After clicking to *Auto Detect* you should see two devices: a *EPM1270* and the FPGAs. The *EPM1270* is the *CPLD for Clock Factory and Configuration* and contains the flash *CFI_128MB*. For this flash choose the generated **.pof* file, check the *Program/Configure* box and click to *Start*. Consequently, the flash is programmed and the FPGAs are configured with the designs after switching off and on the power. However, this method of configuring the FPGAs just works when both chips are configured. It is not possible to configure just one of the FPGAs and leave the other one without configuration.

3.2.2 FPGA Configuration

Due to the fact that the needed configuration signals of the *DUT-FPGA#1* and the *DUT-FPGA#2* are connected to the *CPLD for Clock Factory and Configuration*, it is possible for the user to configure the FPGAs with this system. This is helpful when the *HMX2-AS2* is used as FPGA development platform. The flash is big enough (128 Mbit) to hold the configuration files for the two *EP2S180*. For more information refer to the *Altera* documentation.

If the *SEmulator* is used, it is not possible to configure the FPGA by using the flash because the signals are engaged by the *SEmulator* which configures the FPGA.

3.3 Fan Control

On top of the FPGAs a fan is fixed. The needed voltage (12 V) has to be provided via an extra connector (X7) from the mainboard. The output of the temperature diodes of the FPGAs is connected to the *CPLD for Clock Factory and Configuration* via a temperature sensors. The *CPLD for Clock Factory and Configuration* controls the fans via pulse width modulation (PWM). If the *CPLD for Clock Factory and Configuration* is not configured, the fan runs at full speed.

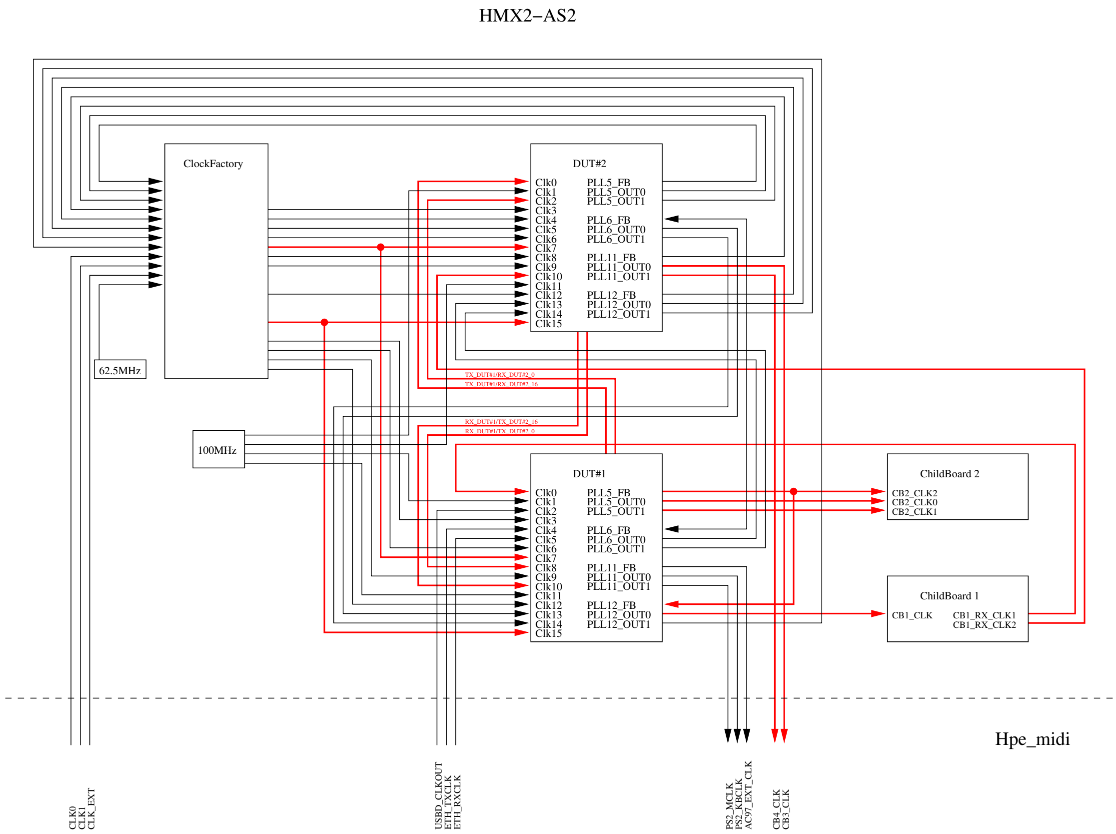


Figure 3.1: The Clock Distribution on the *HMX2-AS2*.

4 CPLD for USB Blaster and FCP

4.1 FCP

The FCP protects the IP core (e.g. the *SEmulator*) within the *DUT-FPGA#1* respectively the *DUT-FPGA#2*. In order to be able to use the advantages of FCP, a black box with the FPGA part of the FCP design has to be ordered. Ask *Gleichmann Electronics Research* for usage.

When using the FCP it is necessary to to switch power off and on and then reconfigure the DUT. That is to say, if the current design is working with the FCP, and FCP should run after reconfiguration as well, switch off the power to your boards, then switch it on again and start with the reconfiguration. If you start to reconfigure the DUTs immediately (without turning off and on the power), the FCP won't work (for security reasons).

4.2 JTAG configuration

The *CPLD for USB Blaster and FCP* also contains the configuration for using the *Altera USB Blaster*. That is to say that only a simple USB cable is necessary to configure the chips on the *HMX2-AS2* via JTAG.

There are two possible ways to use JTAG. The first one is via the *Altera USB Blaster* (on connector X5) and the other way is via the *HC-PCIe*. For using the *Altera USB Blaster* only a simple USB cable is required because the *Altera USB Blaster* is on board on the *HMX2-AS2*.

By default, the JTAG chain consists of three devices:

1. the *CPLD for Clock Factory and Configuration*,
2. the *DUT-FPGA#1* and
3. the *DUT-FPGA#2*.

By default it is not possible to use the *Altera USB Blaster* if the *HC-PCIe* is pluged on the *HMX2-AS2* and connected to the PC (signalled via a high on *CB1_PC_CON* and the blue LED *PC* in the middle of the box named *ComCon*). In this case the JTAG chain can only be reached via PCI Express and the *Communication Controller*.

Moreover, it is possible to integrate an own JTAG core into the customer design (which is in the *DUT-FPGA#1* and/or the *DUT-FPGA#2*) and put it into the JTAG chain. Therefore the *HC-PCIe* is needed. If the signal *CB1_SEL_DUT_JTAG* is driven low by the *Communication Controller*, the JTAG chain consists of five devices:

1. the *CPLD for Clock Factory and Configuration*,
2. the *DUT-FPGA#1*,
3. the *DUT-FPGA#1*,
4. the internal JTAG design of *DUT-FPGA#1* and
5. the internal JTAG design of *DUT-FPGA#2*.

By a resistor jumper—stuff R0627 and R0628 instead of R0630 with 0 ohm resistors—it is possible to loop the JTAG chain to the mainboard. This is advantageous if there is a device on the mainboard that should be in the chain as well. By now, the JTAG chain looks like this:

1. the *CPLD for Clock Factory and Configuration*,
2. the chips on the mainboard,
3. the *DUT-FPGA#1*,
4. the *DUT-FPGA#2* and
5. optional an internal JTAG design of *DUT-FPGA#1* and *DUT-FPGA#2*.

4.3 Connection to the CPLD for Clock Factory and Configuration

A bus of 34 bits connects the *CPLD for USB Blaster and FCP* with the *CPLD for Clock Factory and Configuration*. This bus is reserved for internal use.

5 Elastomer Connectors

5.1 Module Connectors

The *HMX2-AS2* is connected to the mainboard via the elastomer module connectors (X1 and X2). Below you find a brief summary of the most important pins. For more detailed information refer to the manual of the *Hpe_midi*.

5.1.1 JTAG

Five signals are reserved for JTAG configuration:

- Test Data Input (TDI)
- Test Data Output (TDO)
- Test ClocK (TCK)
- Test Mode Select Input (TMS)
- Test ReSeT (TRST)

By default there is no JTAG connection available between the *HMX2-AS2* and the mainboard because usually there is no configurable chip on the mainboard. However, if it is necessary, there is a possibility to expand the JTAG chain to the mainboard. By a resistor jumper—stuff R0627 and R0628 instead of R0630 with 0 ohm resistors—it is possible to loop the JTAG chain to the mainboard. Now one or more devices on the mainboard are in the chain as well. The JTAG chain is made up by the chips on the *HMX2-AS2* (*CPLD for Clock Factory and Configuration*, *DUT-FPGA#1* and *DUT-FPGA#2*) and by the chips on the mainboard.

5.1.2 Global Reset

There is one system wide reset (*PWR_RESET#*) which resets all CPLDs and FPGAs on the *HMX2-AS2*. The reset is low active, activated after power up and controlled by a supervisor on the *Hpe_midi*.

5.1.3 Clocks

Three clocks (two from a socket and one from external) are delivered from the mainboard via the connectors to the *CPLD for Clock Factory and Configuration*.

5.1.4 Power Control

5 V and 3.3 V are delivered via the two elastomer module connectors. Additionally, three signals are reserved for power control. This feature is not used at the moment.

5.1.5 I/Os for Peripherals

In sum there are 473 I/O signals available between the the connectors and *DUT-FPGA#1* respectively *DUT-FPGA#2*. The *HMX2-AS2* is compatible with the mainboard *Hpe_midi*.

5.2 Hpe_Childboard Connectors

The *HMX2-AS2* is featured with two *Hpe_childboard* connectors. The *Hpe_childboard* is used to add additional hardware or interfaces to the *HMX2-AS2*. The *Hpe_childboard* 1 on connector X3 can handle LVDS signals and can be used for the *HC-PCIe* in order to be able to use the *SEmulator* engine. This *Hpe_childboard* connector can also be used for most other *Hpe_childboards*. However, not all pins are connected to the *DUT-FPGA#1* respectively the *DUT-FPGA#2*. Refer to section 5.2.1 for more details.

The *Hpe_childboard* 2 on connector can be used for all *Hpe_childboard* but the *HC-PCIe*. It is completely connected to the *DUT-FPGA#1*.

5.2.1 Hpe_Childboard 1

This *Hpe_childboard* can be used for LVDS signals and is especially prepared for the *SEmulator* .

This connector (X3) has the purpose to handle nearly all *Hpe_childboards* which work with up to 85 I/O pins. Beside that, it has the feature of 16 LVDS receiver pairs and 16 LVDS transmitter pairs. By default, all I/O signals work with a power supply of 2.5 V. However, this I/O voltage can be changed to 3.3 V by setting the signal *CB1_SEL_LVDS_VAL* to low. This signal is controlled by the *Hpe_childboard*. As usual 3.3 V are delivered to the *Hpe_childboard* via the connector. Additionally, 2.5 V are delivered to the *Hpe_childboard* as well.

In table 5.1 and 5.2 you find the pin connection for this *Hpe_childboard*. The signal names are for a *Hpe_childboard* with *Communication Controller* and PCI Express (*HC-PCIe*). Nevertheless, most of the signals can be used as regular I/Os as well and only the *emphasised* ones do not have a connection to the an I/O pin on the *DUT-FPGA#1* respectively the *DUT-FPGA#2*.

The *emphasised* signals have the following meaning:

- *CB1_SEL_LVDS_VAL:* Pulled to low (or left floating) causes 2.5 V I/O supply on the signals pins of the *DUT-FPGA#1* respectively the *DUT-FPGA#2* which are connected to the *Hpe_childboard* 1. Driven high causes 3.3 V I/O supply voltage on these pins.
- *CB1_CONF_DONE:* Needed for configuring the DUTs.
- *CB1_STATUS#:* Needed for configuring the DUTs.
- *CB1_DCLK:* Needed for configuring the DUTs.
- *CB1_CONFIG#:* Needed for configuring the DUTs.
- *CB1_SEL_DUT_JTAG:* If this pin is driven low, it is possible to put an own JTAG core into the JTAG chain.
- *CB1_CC_READY:* Connected to a LED, signals that the *Communication Controller* is prepared.
- *CB1_DATA:* Connected to a LED, signals that the *Communication Controller* is transmitting/receiving data.
- *CB1_PC_CON:* Connected to a LED, signals that the *Communication Controller* is connected to the PC via PCI Express.
- *CB1_FAN:* Connected to a LED, signals that fan for the *Communication Controller* is activated.
- *CB1_TDO:* JTAG pin (test data out), needed for the configuration of *Clock Factory* and DUTs via *Hpe_childboard*.

Odd Side A			*Even Side A*		
Pin Number	*Signal Name*	*DUT*	*Pin Number*	*Signal Name*	*DUT*
A1	CB1_RX_CLK1+	*DUT#1*	A2	CB1_TX_CLK1+	*DUT#1*
A3	CB1_RX_CLK1-	*DUT#1*	A4	CB1_TX_CLK1-	*DUT#1*
A5	CB1_RX_01+	*DUT#1*	A6	CB1_TX_01+	*DUT#1*
A7	CB1_RX_01-	*DUT#1*	A8	CB1_TX_01-	*DUT#1*
A9	CB1_RX_02+	*DUT#1*	A10	CB1_TX_02+	*DUT#1*
A11	CB1_RX_02-	*DUT#1*	A12	CB1_TX_02-	*DUT#1*
A13	CB1_RX_03+	*DUT#1*	A14	CB1_TX_03+	*DUT#1*
A15	CB1_RX_03-	*DUT#1*	A16	CB1_TX_03-	*DUT#1*
A17	CB1_RX_CLK2+	*DUT#2*	A18	CB1_TX_CLK2+	*DUT#2*
A19	CB1_RX_CLK2-	*DUT#2*	A20	CB1_TX_CLK2-	*DUT#2*
A21	CB1_RX_04+	*DUT#2*	A22	CB1_TX_04+	*DUT#2*
A23	CB1_RX_04-	*DUT#2*	A24	CB1_TX_04-	*DUT#2*
A25	CB1_RX_05+	*DUT#2*	A26	CB1_TX_05+	*DUT#2*
A27	CB1_RX_05-	*DUT#2*	A28	CB1_TX_05-	*DUT#2*
A29	CB1_RX_06+	*DUT#2*	A30	CB1_TX_06+	*DUT#2*
A31	CB1_RX_06-	*DUT#2*	A32	CB1_TX_06-	*DUT#2*
A33	VCC3V3	—	A34	GND	—
A35	VCC3V3	—	A36	GND	—
A37	VCC3V3	—	A38	GND	—
A39	VCC3V3	—	A40	GND	—
A41	VCC3V3	—	A42	GND	—
A43	VCC3V3	—	A44	GND	—
A45	VCC3V3	—	A46	GND	—
A47	VCC3V3	—	A48	GND	—
A49	CB1_CLK+	*DUT#1*	A50	CB1_CLK-	*DUT#1*
A51	GND	—	A52	GND	—
A53	CB1_DATA0	*DUT#1*	A54	CB1_DATA7	*DUT#1*
A55	CB1_DATA1	*DUT#1*	A56	*CB1_CONF_DONE*	—
A57	CB1_DATA2	*DUT#1*	A58	*CB1_STATUS#*	—
A59	CB1_DATA3	*DUT#1*	A60	*CB1_DCLK*	—
A61	CB1_DATA4	*DUT#1*	A62	*CB1_CONFIG#*	—
A63	CB1_DATA5	*DUT#1*	A64	*CB1_CC_READY*	—
A65	CB1_DATA6	*DUT#1*	A66	*CB1_SEL_DUT_JTAG*	—

Table 5.1: Pin connection for *Hpe_childboard* 1, side A

- *CB1_TDI:* JTAG pin (test data in), needed for the configuration of *Clock Factory* and DUTs via *Hpe_childboard*.
- *CB1_TMS:* JTAG pin (test mode select), needed for the configuration of *Clock Factory* and DUTs via *Hpe_childboard*.
- *CB1_TCK:* JTAG pin (test clock), needed for the configuration of *Clock Factory* and DUTs via *Hpe_childboard*.

Be aware that you probably manipulate the signals *DATA_BUS374* to *DATA_BUS501* between the two FGPAs when using the signals *CB1_TEST[*]* and *CB1_EN_TEST#[*]*. Refer to section 7.8.4

5.2.2 Hpe_Childboard 2

This connector (X4) has the purpose to handle nearly all *Hpe_childboards* which work with up to 99 I/O pins. It is connected to the *DUT-FPGA#2*. As usual 3.3 V are delivered to the *Hpe_childboard* via the connector. Whenever a power supply higher than 1.5 V and lower

Odd Side B			Even Side B		
Pin Number	*Signal Name*	*DUT*	*Pin Number*	*Signal Name*	*DUT*
B1	CB1_RX_CLK3+	*DUT#1*	B2	CB1_TX_CLK3+	*DUT#1*
B3	CB1_RX_CLK3-	*DUT#1*	B4	CB1_TX_CLK3-	*DUT#1*
B5	CB1_RX_07+	*DUT#1*	B6	CB1_TX_07+	*DUT#1*
B7	CB1_RX_07-	*DUT#1*	B8	CB1_TX_07-	*DUT#1*
B9	CB1_RX_08+	*DUT#1*	B10	CB1_TX_08+	*DUT#1*
B11	CB1_RX_08-	*DUT#1*	B12	CB1_TX_08-	*DUT#1*
B13	CB1_RX_09+	*DUT#1*	B14	CB1_TX_09+	*DUT#1*
B15	CB1_RX_09-	*DUT#1*	B16	CB1_TX_09-	*DUT#1*
B17	CB1_RX_CLK4+	*DUT#1*	B18	CB1_TX_CLK4+	*DUT#1*
B19	CB1_RX_CLK4-	*DUT#1*	B20	CB1_TX_CLK4-	*DUT#1*
B21	CB1_RX_10+	*DUT#1*	B22	CB1_TX_10+	*DUT#1*
B23	CB1_RX_10-	*DUT#1*	B24	CB1_TX_10-	*DUT#1*
B25	CB1_RX_11+	*DUT#1*	B26	CB1_TX_11+	*DUT#1*
B27	CB1_RX_11-	*DUT#1*	B28	CB1_TX_11-	*DUT#1*
B29	CB1_RX_12+	*DUT#1*	B30	CB1_TX_12+	*DUT#1*
B31	CB1_RX_12-	*DUT#1*	B32	CB1_TX_12-	*DUT#1*
B33	VCC2V5	—	B34	*CB1_SEL_LVDS_VAL*	—
B35	VCC2V5	—	B36	GND	—
B37	VCC2V5	—	B38	GND	—
B39	VCC2V5	—	B40	GND	—
B41	VCC2V5	—	B42	GND	—
B43	VCC2V5	—	B44	GND	—
B45	VCC2V5	—	B46	GND	—
B47	VCC2V5	—	B48	GND	—
B49	*CB1_DATA*	—	B50	*CB1_PC_CON*	—
B51	*CB1_TDO*	—	B52	*CB1_TDI*	—
B53	*CB1_TMS*	—	B54	*CB1_TCK*	—
B55	*CB1_FAN*	—	B56	CB1_TEST0	*DUT#1*
B57	CB1_TEST1	*DUT#1*	B58	CB1_TEST2	*DUT#1*
B59	CB1_TEST3	*DUT#1*	B60	CB1_EN_TEST#0	*DUT#1*
B61	CB1_EN_TEST#1	*DUT#1*	B62	CB1_EN_TEST#2	*DUT#1*
B63	CB1_EN_TEST#3	*DUT#1*	B64	CB1_RFU0	*DUT#1*
B65	CB1_RFU1	*DUT#1*	B66	CB1_RFU2	*DUT#1*

Table 5.2: Pin connection for *Hpe_childboard* 1, side B

than 3.3 V on the *VCCVAR1* pins is available, a power multiplexer switches the *VCCVAR1* to the VCCIO pins on the *DUT-FPGA#2* that need these voltages in order to handle the signals connected the the *Hpe_childboard* with the delivered voltage. By default these pins are delivered with 3.3 V.

VCCVAR2 is connected to the corresponding VREF pins. By default thes VREF pins are connected to ground.

In table 5.3 and 5.4 you find the pin connection for this *Hpe_childboard*.

Odd Side A		Even Side A	
Pin Number	*Signal Name*	*Pin Number*	*Signal Name*
A1	CB2_BUS[0]	A2	CB2_BUS[1]
A3	CB2_BUS[2]	A4	CB2_BUS[3]
A5	CB2_BUS[4]	A6	CB2_BUS[5]
A7	CB2_BUS[6]	A8	CB2_BUS[7]
A9	CB2_BUS[8]	A10	CB2_BUS[9]
A11	CB2_BUS[10]	A12	CB2_BUS[11]
A13	CB2_BUS[12]	A14	CB2_BUS[13]
A15	CB2_BUS[14]	A16	CB2_BUS[15]
A17	CB2_BUS[16]	A18	CB2_BUS[17]
A19	CB2_BUS[18]	A20	CB2_BUS[19]
A21	CB2_BUS[20]	A22	CB2_BUS[21]
A23	CB2_BUS[22]	A24	CB2_BUS[23]
A25	CB2_BUS[24]	A26	CB2_BUS[25]
A27	CB2_BUS[26]	A28	CB2_BUS[27]
A29	CB2_BUS[28]	A30	CB2_BUS[29]

Odd Side B		*Even Side B*	
Pin Number	*Signal Name*	*Pin Number*	*Signal Name*
B1	CB2_BUS[32]	B2	CB2_BUS[33]
B3	CB2_BUS[34]	B4	CB2_BUS[35]
B5	CB2_BUS[36]	B6	CB2_BUS[37]
B7	CB2_BUS[38]	B8	CB2_BUS[39]
B9	CB2_BUS[40]	B10	CB2_BUS[41]
B11	CB2_BUS[42]	B12	CB2_BUS[43]
B13	CB2_BUS[44]	B14	CB2_BUS[45]
B15	CB2_BUS[46]	B16	CB2_BUS[47]
B17	CB2_BUS[48]	B18	CB2_BUS[49]
B19	CB2_BUS[50]	B20	CB2_BUS[51]
B21	CB2_BUS[52]	B22	CB2_BUS[53]
B23	CB2_BUS[54]	B24	CB2_BUS[55]
B25	CB2_BUS[56]	B26	CB2_BUS[57]
B27	CB2_BUS[58]	B28	CB2_BUS[59]
B29	CB2_BUS[60]	B30	CB2_BUS[61]
B31	CB2_BUS[62]	B32	CB2_BUS[63]
B33	VCCVAR1	B34	CB2_IO[14]
B35	VCCVAR1	B36	GND
B37	VCCVAR1	B38	GND
B39	VCCVAR1	B40	GND
B41	VCCVAR2	B42	GND
B43	VCCVAR2	B44	GND
B45	VCCVAR2	B46	GND
B47	VCCVAR2	B48	GND
B49	CB2_IO[15]	B50	CB2_IO[16]
B51	CB2_IO[17]	B52	CB2_IO[18]
B53	CB2_IO[19]	B54	CB2_IO[20]
B55	CB2_IO[21]	B56	CB2_IO[22]
B57	CB2_IO[23]	B58	CB2_IO[24]
B59	CB2_IO[25]	B60	CB2_IO[26]
B61	CB2_IO[27]	B62	CB2_IO[28]
B63	CB2_IO[29]	B64	CB2_IO[30]
B65	CB2_IO[31]	B66	CB2_IO[32]

Table 5.4: Pin connection for *Hpe_childboard* 2.

6 Power Supply

6.1 Power Source

In order to be able to work with the *HMX2-AS2* the mainboard (*Hpe_midi*) is necessary. The mainboard provides the connection, the clocks and the power supply for many peripherals. For a accurate operation of the *HMX2-AS2* two voltages are needed, 5 V and 3.3 V. These voltages are delivered via the two elastomer module connectors (X1, X2).

For the fan, the needed voltage (12 V) has to be provided by an extra connector (X7).

6.2 Generated Power

On the *HMX2-AS2* 2.5 V (for LVDS) and two times 1.2 V (core voltages) are generated out of the two given voltages. When you look at the front side of your *SEmulator* engine, a box named *Power* can be seen. The first LED in this box is green and signals power good for the 2.5 V. The second LED in the box named *Power* (which is green as well) signals power good for the core voltage of *DUT-FPGA#1* and the third LED in this box signals power good for the core voltage of *DUT-FPGA#2*. .

6.3 I/O Power

6.3.1 I/O Power on DUT#1

The signals of the bank 1, 2, 4 and 7 are solely connected to the *DUT-FPGA#2* and therefore supplied with 2.5 V.

The signals of bank 3 are connected to the *Hpe_childboard* 2, which can be used with different I/O voltages. By default this bank is delivered with 3.3 V. However, the power supply can change to a various voltage between 1.5 V and 3.3 V. Since this various voltage is not generated on the *HMX2-AS2*, the *Hpe_childboard* 2 has to deliver it. *VCCVAR1* and *VCCVAR2* (reference voltage) have to be generated on the *Hpe_childboard* out of the delivered 3.3 V (refer to section 5.2.2). As soon a valid voltage is received from the *Hpe_childboard* on X4, the power supply for bank 3 switches from 3.3 V to the given voltage.

Bank 5, which is connected to the *Hpe_childboard* 1, is delivered with 2.5 V by default. The signals on this bank can handle the LVDS standard. Only if the signal *B43—CB1_SEL_LVDS_VAL* is driven low, also bank 5 is delivered with 3.3 V (refer to section 5.2.1). Be aware of the fact that it is only possible to use LVDS, when a supply voltage of 2.5 V is available.

The signals of the FPGA-banks 6 and 8 are solely connected to the mainboard. These banks are supplied with 3.3 V.

6.3.2 I/O Power on DUT#2

The signals of the bank 1, 2, 3, 4 and 6 are solely connected to the *DUT-FPGA#1* and therefore supplied with 2.5 V.

Bank 5, which is connected to the *Hpe_childboard* 1, is delivered with 2.5 V by default. The signals on this bank can handle the LVDS standard. Only if the signal *B43—CB1_SEL_LVDS_VAL* is driven low, also bank 5 is delivered with 3.3 V (refer to section 5.2.1). Be aware of the fact that it is only possible to use LVDS, when a supply voltage of 2.5 V is available.

Bank 7 and 8 are supplied with 3.3 V since the pins on this bank are connected to the mainboard.

7 FPGA DUT#1

You find a file with the lengths of all signals on your data disc.

Generally, all signals named **-* and **+* are differential signals where only the signal named **+* is addressed when using the LVDS standard. However, if the signal is used in a single ended standard, both **-* and **+* can be used independently.

A signal with a # in its name is low active.

7.1 PLLs

PLL 5 is driven with 2.5 V by default. However, if it is necessary (e.g. for LVDS clocks) there is the possibility to change the power supply to 3.3 V via a resistor jumper (stuff RJ14 instead of RJ13 with a 0 ohm resistor).

PLL 6 is driven with 3.3 V by default. However, if a *Hpe_childboard* with a different voltage is stuck, it is driven with the delivered voltage. If it is needed to supply the PLL 6 with 3.3 V in spite of the fact that an other voltage delivered from the *Hpe_childboard*, this is possible by stuffing RJ16 instead of RJ15 with a 0 ohm resistor.

PLL 11 is always supplied with 3.3 V.

PLL 12 is (like PLL 6) delivered with 3.3 V, respectively the delivered voltage if a *Hpe_childboard* with another voltage is stuck. This is true, when RJ17 is stuffed (this is done by default). Additionally, it is possible to stuff RJ18 instead of RJ17 with a 0 ohm resistor. Consequently, it is possible to choise between two other power supplies. If RJ19 is stuffed (this is done by default) in addition to RJ18, PLL 12 is delivered with 2.5 V by default. However, the voltage can be switched to 3.3 V by driving *CB1_SEL_LVDS_VAL* on *Hpe_childboard* with low. If RJ20 is stuffed with a 0 ohm resistor in addition to RJ18, the PLL is supplied with 3.3 V.

Please contact *Gleichmann Electronics Research* for further details where to find the RJs.

7.2 Connection to DUT-FPGA#2

A bus of 512 bits width is established between the two DUT-FGPAs. It is possible to measure high-impedance ('Z') on 128 lines of this bus. Additionally, a LVDS connection of 32 differential pairs per direction is available.

The 512 bit bus works with an I/O supply of 2.5 V. However, on *DUT-FPGA#1* two signals are driven with 3.3 V: *DATA_BUS500* and *DATA_BUS501*.

In table 7.1 the 512-bit bus connection to *DUT-FPGA#2* can be found. The signals, on which a 'Z' measuring is possible are *emphasised*.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
DATA_BUS[0]	IO_VB6N2_AD6	AD6
DATA_BUS[1]	IO_VB6N2_AD7	AD7
DATA_BUS[2]	IO_VB6N2_AE5	AE5
DATA_BUS[3]	IO_VB6N2_AE6	AE6
DATA_BUS[4]	IO_VB6N2_AE7	AE7
DATA_BUS[5]	IO_VB6N2_AE8	AE8
DATA_BUS[6]	IO_VB6N2_AE9	AE9

DATA_BUS[7]	IO_VB6N2_AE10	AE10
DATA_BUS[8]	IO_VB6N2_AE11	AE11
DATA_BUS[9]	IO_VB6N2_AE12	AE12
DATA_BUS[10]	IO_VB6N2_AF5	AF5
DATA_BUS[11]	IO_VB6N2_AF6	AF6
DATA_BUS[12]	IO_VB6N2_AF7	AF7
DATA_BUS[13]	IO_VB6N2_AF8	AF8
DATA_BUS[14]	IO_VB6N2_AF10	AF10
DATA_BUS[15]	IO_VB6N2_AF11	AF11
DATA_BUS[16]	IO_VB6N2_AG6	AG6
DATA_BUS[17]	IO_VB6N2_AG7	AG7
DATA_BUS[18]	IO_VB6N2_AH3	AH3
DATA_BUS[19]	IO_VB6N2_AH4	AH4
DATA_BUS[20]	IO_VB6N2_AH5	AH5
DATA_BUS[21]	IO_VB6N2_AH6	AH6
DATA_BUS[22]	IO_VB6N2_AJ3	AJ3
DATA_BUS[23]	IO_VB6N2_AJ4	AJ4
DATA_BUS[24]	IO_VB6N2_AK3	AK3
DATA_BUS[25]	IO_VB6N2_AK4	AK4
DATA_BUS[26]	IO_VB6N2_AL1	AL1
DATA_BUS[27]	IO_VB6N2_AL2	AL2
DATA_BUS[28]	IO_VB6N2_AL3	AL3
DATA_BUS[29]	IO_VB6N2_AL4	AL4
DATA_BUS[30]	IO_VB6N2_AM1	AM1
DATA_BUS[31]	IO_VB6N2_AM2	AM2
DATA_BUS[32]	IO_VB6N1_AD13	AD13
DATA_BUS[33]	IO_VB6N1_AD14	AD14
DATA_BUS[34]	IO_VB6N1_AE13	AE13
DATA_BUS[35]	IO_VB6N1_AE14	AE14
DATA_BUS[36]	IO_VB6N1_AF12	AF12
DATA_BUS[37]	IO_VB6N1_AF13	AF13
DATA_BUS[38]	IO_VB6N1_AG8	AG8
DATA_BUS[39]	IO_VB6N1_AG9	AG9
DATA_BUS[40]	IO_VB6N1_AG10	AG10
DATA_BUS[41]	IO_VB6N1_AG11	AG11
DATA_BUS[42]	IO_VB6N1_AG12	AG12
DATA_BUS[43]	IO_VB6N1_AG13	AG13
DATA_BUS[44]	IO_VB6N1_AH7	AH7
DATA_BUS[45]	IO_VB6N1_AH8	AH8
DATA_BUS[46]	IO_VB6N1_AH9	AH9
DATA_BUS[47]	IO_VB6N1_AH10	AH10
DATA_BUS[48]	IO_VB6N1_AH11	AH11
DATA_BUS[49]	IO_VB6N1_AH12	AH12
DATA_BUS[50]	IO_VB6N1_AJ5	AJ5
DATA_BUS[51]	IO_VB6N1_AJ6	AJ6
DATA_BUS[52]	IO_VB6N1_AK5	AK5
DATA_BUS[53]	IO_VB6N1_AK6	AK6
DATA_BUS[54]	IO_VB6N1_AL5	AL5
DATA_BUS[55]	IO_VB6N1_AL6	AL6
DATA_BUS[56]	IO_VB6N1_AM3	AM3
DATA_BUS[57]	IO_VB6N1_AM4	AM4

DATA_BUS[58]	IO_VB6N1_AN1	AN1
DATA_BUS[59]	IO_VB6N1_AN2	AN2
DATA_BUS[60]	IO_VB6N1_AN3	AN3
DATA_BUS[61]	IO_VB6N1_AN4	AN4
DATA_BUS[62]	IO_VB6N1_AP1	AP1
DATA_BUS[63]	IO_VB6N1_AP2	AP2
DATA_BUS[64]	IO_VB6N1_AR1	AR1
DATA_BUS[65]	IO_VB6N1_AR2	AR2
DATA_BUS[66]	IO_VB6N1_AV2	AV2
DATA_BUS[67]	IO_VB6N1_AV3	AV3
DATA_BUS[68]	IO_VB6N0_AJ7	AJ7
DATA_BUS[69]	IO_VB6N0_AJ8	AJ8
DATA_BUS[70]	IO_VB6N0_AJ9	AJ9
DATA_BUS[71]	IO_VB6N0_AJ10	AJ10
DATA_BUS[72]	IO_VB6N0_AK8	AK8
DATA_BUS[73]	IO_VB6N0_AK9	AK9
DATA_BUS[74]	IO_VB6N0_AL8	AL8
DATA_BUS[75]	IO_VB6N0_AL9	AL9
DATA_BUS[76]	IO_VB6N0_AM5	AM5
DATA_BUS[77]	IO_VB6N0_AM6	AM6
DATA_BUS[78]	IO_VB6N0_AM8	AM8
DATA_BUS[79]	IO_VB6N0_AM9	AM9
DATA_BUS[80]	IO_VB6N0_AN6	AN6
DATA_BUS[81]	IO_VB6N0_AN7	AN7
DATA_BUS[82]	IO_VB6N0_AP3	AP3
DATA_BUS[83]	IO_VB6N0_AP4	AP4
DATA_BUS[84]	IO_VB6N0_AP5	AP5
DATA_BUS[85]	IO_VB6N0_AP6	AP6
DATA_BUS[86]	IO_VB6N0_AR3	AR3
DATA_BUS[87]	IO_VB6N0_AR4	AR4
DATA_BUS[88]	IO_VB6N0_AR5	AR5
DATA_BUS[89]	IO_VB6N0_AR6	AR6
DATA_BUS[90]	IO_VB6N0_AT3	AT3
DATA_BUS[91]	IO_VB6N0_AT4	AT4
DATA_BUS[92]	IO_VB6N0_AU3	AU3
DATA_BUS[93]	IO_VB6N0_AU4	AU4
DATA_BUS[94]	IO_VB5N4_C3	C3
DATA_BUS[95]	IO_VB5N4_C4	C4
DATA_BUS[96]	IO_VB5N4_J8	J8
DATA_BUS[97]	IO_VB5N4_J9	J9
DATA_BUS[98]	IO_VB5N4_L9	L9
DATA_BUS[99]	IO_VB5N4_L10	L10
DATA_BUS[100]	IO_VB5N3_B2	B2
DATA_BUS[101]	IO_VB5N3_B3	B3
DATA_BUS[102]	IO_VB5N3_D3	D3
DATA_BUS[103]	IO_VB5N3_D4	D4
DATA_BUS[104]	IO_VB5N3_E1	E1
DATA_BUS[105]	IO_VB5N3_E2	E2
DATA_BUS[106]	IO_VB5N3_E3	E3
DATA_BUS[107]	IO_VB5N3_E4	E4
DATA_BUS[108]	IO_VB5N3_E5	E5

DATA_BUS[109]	IO_VB5N3_E6	E6
DATA_BUS[110]	IO_VB5N3_F3	F3
DATA_BUS[111]	IO_VB5N3_F4	F4
DATA_BUS[112]	IO_VB5N3_F5	F5
DATA_BUS[113]	IO_VB5N3_F6	F6
DATA_BUS[114]	IO_VB5N3_G5	G5
DATA_BUS[115]	IO_VB5N3_G6	G6
DATA_BUS[116]	IO_VB5N3_H5	H5
DATA_BUS[117]	IO_VB5N3_H6	H6
DATA_BUS[118]	IO_VB5N3_H8	H8
DATA_BUS[119]	IO_VB5N3_H9	H9
DATA_BUS[120]	IO_VB5N3_J6	J6
DATA_BUS[121]	IO_VB5N3_J7	J7
DATA_BUS[122]	IO_VB5N3_K5	K5
DATA_BUS[123]	IO_VB5N3_K6	K6
DATA_BUS[124]	IO_VB5N3_K8	K8
DATA_BUS[125]	IO_VB5N3_K9	K9
DATA_BUS[126]	IO_VB5N3_L7	L7
DATA_BUS[127]	IO_VB5N3_L8	L8
DATA_BUS[128]	IO_VB5N3_M7	M7
DATA_BUS[129]	IO_VB5N3_M8	M8
DATA_BUS[130]	IO_VB5N3_M9	M9
DATA_BUS[131]	IO_VB5N3_M10	M10
DATA_BUS[132]	IO_VB5N3_M11	M11
DATA_BUS[133]	IO_VB5N3_M12	M12
DATA_BUS[134]	IO_VB5N3_N9	N9
DATA_BUS[135]	IO_VB5N3_N10	N10
DATA_BUS[136]	IO_VB5N2_J3	J3
DATA_BUS[137]	IO_VB5N2_J4	J4
DATA_BUS[138]	IO_VB5N2_K3	K3
DATA_BUS[139]	IO_VB5N2_K4	K4
DATA_BUS[140]	IO_VB5N2_L3	L3
DATA_BUS[141]	IO_VB5N2_L4	L4
DATA_BUS[142]	IO_VB5N2_L5	L5
DATA_BUS[143]	IO_VB5N2_L6	L6
DATA_BUS[144]	IO_VB5N2_M3	M3
DATA_BUS[145]	IO_VB5N2_M4	M4
DATA_BUS[146]	IO_VB5N2_M5	M5
DATA_BUS[147]	IO_VB5N2_M6	M6
DATA_BUS[148]	IO_VB5N2_N5	N5
DATA_BUS[149]	IO_VB5N2_N6	N6
DATA_BUS[150]	IO_VB5N2_N7	N7
DATA_BUS[151]	IO_VB5N2_N8	N8
DATA_BUS[152]	IO_VB5N2_N11	N11
DATA_BUS[153]	IO_VB5N2_N12	N12
DATA_BUS[154]	IO_VB5N2_P7	P7
DATA_BUS[155]	IO_VB5N2_P8	P8
DATA_BUS[156]	IO_VB5N2_P9	P9
DATA_BUS[157]	IO_VB5N2_P10	P10
DATA_BUS[158]	IO_VB5N2_P11	P11
DATA_BUS[159]	IO_VB5N2_P12	P12

DATA_BUS[160]	IO_VB5N2_P13	P13
DATA_BUS[161]	IO_VB5N2_P14	P14
DATA_BUS[162]	IO_VB5N2_R8	R8
DATA_BUS[163]	IO_VB5N2_R9	R9
DATA_BUS[164]	IO_VB5N2_F1	F1
DATA_BUS[165]	IO_VB5N2_F2	F2
DATA_BUS[166]	IO_VB5N2_G1	G1
DATA_BUS[167]	IO_VB5N2_G2	G2
DATA_BUS[168]	IO_VB5N2_G3	G3
DATA_BUS[169]	IO_VB5N2_G4	G4
DATA_BUS[170]	IO_VB5N2_H3	H3
DATA_BUS[171]	IO_VB5N2_H4	H4
DATA_BUS[172]	IO_VB4N4_A17	A17
DATA_BUS[173]	IO_VB4N4_B16	B16
DATA_BUS[174]	IO_VB4N4_B17	B17
DATA_BUS[175]	IO_VB4N4_C16	C16
DATA_BUS[176]	IO_VB4N4_C17	C17
DATA_BUS[177]	IO_VB4N4_D16	D16
DATA_BUS[178]	IO_VB4N4_D17	D17
DATA_BUS[179]	IO_VB4N4_E16	E16
DATA_BUS[180]	IO_VB4N4_F19	F19
DATA_BUS[181]	IO_VB4N4_G20	G20
DATA_BUS[182]	IO_VB4N4_H19	H19
DATA_BUS[183]	IO_VB4N4_H20	H20
DATA_BUS[184]	IO_VB4N4_J18	J18
DATA_BUS[185]	IO_VB4N4_M19	M19
DATA_BUS[186]	IO_VB4N2_A10	A10
DATA_BUS[187]	IO_VB4N2_A11	A11
DATA_BUS[188]	IO_VB4N3_A14	A14
DATA_BUS[189]	IO_VB4N3_A15	A15
DATA_BUS[190]	IO_VB4N3_B14	B14
DATA_BUS[191]	IO_VB4N3_B15	B15
DATA_BUS[192]	IO_VB4N3_C13	C13
DATA_BUS[193]	IO_VB4N3_C14	C14
DATA_BUS[194]	IO_VB4N3_C15	C15
DATA_BUS[195]	IO_VB4N3_D13	D13
DATA_BUS[196]	IO_VB4N3_D14	D14
DATA_BUS[197]	IO_VB4N3_D15	D15
DATA_BUS[198]	IO_VB4N3_E13	E13
DATA_BUS[199]	IO_VB4N3_E14	E14
DATA_BUS[200]	IO_VB4N3_E15	E15
DATA_BUS[201]	IO_VB4N3_F13	F13
DATA_BUS[202]	IO_VB4N3_F14	F14
DATA_BUS[203]	IO_VB4N3_F16	F16
DATA_BUS[204]	IO_VB4N3_F18	F18
DATA_BUS[205]	IO_VB4N3_G19	G19
DATA_BUS[206]	IO_VB4N3_H17	H17
DATA_BUS[207]	IO_VB4N3_H18	H18
DATA_BUS[208]	IO_VB4N3_J16	J16
DATA_BUS[209]	IO_VB4N3_J17	J17
DATA_BUS[210]	IO_VB4N3_K17	K17

DATA_BUS[211]	IO_VB4N3_L18	L18
DATA_BUS[212]	IO_VB4N3_N19	N19
DATA_BUS[213]	IO_VB4N4_N20	N20
DATA_BUS[214]	IO_VB4N4_P20	P20
DATA_BUS[215]	IO_VB4N2_A12	A12
DATA_BUS[216]	IO_VB4N2_A13	A13
DATA_BUS[217]	IO_VB4N2_B10	B10
DATA_BUS[218]	IO_VB4N2_B11	B11
DATA_BUS[219]	IO_VB4N2_B12	B12
DATA_BUS[220]	IO_VB4N2_B13	B13
DATA_BUS[221]	IO_VB4N2_C11	C11
DATA_BUS[222]	IO_VB4N2_C12	C12
DATA_BUS[223]	IO_VB4N2_D11	D11
DATA_BUS[224]	IO_VB4N2_D12	D12
DATA_BUS[225]	IO_VB4N2_E11	E11
DATA_BUS[226]	IO_VB4N2_E12	E12
DATA_BUS[227]	IO_VB4N2_G16	G16
DATA_BUS[228]	IO_VB4N2_G17	G17
DATA_BUS[229]	IO_VB4N2_G18	G18
DATA_BUS[230]	IO_VB4N2_H15	H15
DATA_BUS[231]	IO_VB4N2_H16	H16
DATA_BUS[232]	IO_VB4N2_J14	J14
DATA_BUS[233]	IO_VB4N2_J15	J15
DATA_BUS[234]	IO_VB4N2_K15	K15
DATA_BUS[235]	IO_VB4N2_K16	K16
DATA_BUS[236]	IO_VB4N2_L16	L16
DATA_BUS[237]	IO_VB4N2_L17	L17
DATA_BUS[238]	IO_VB4N2_M17	M17
DATA_BUS[239]	IO_VB4N2_M18	M18
DATA_BUS[240]	IO_VB4N2_N17	N17
DATA_BUS[241]	IO_VB4N2_N18	N18
DATA_BUS[242]	IO_VB4N1_N16	N16
DATA_BUS[243]	IO_VB4N0_K12	K12
DATA_BUS[244]	IO_VB4N0_K13	K13
DATA_BUS[245]	IO_VB4N1_A9	A9
DATA_BUS[246]	IO_VB4N1_B7	B7
DATA_BUS[247]	IO_VB4N1_B8	B8
DATA_BUS[248]	IO_VB4N1_B9	B9
DATA_BUS[249]	IO_VB4N1_C7	C7
DATA_BUS[250]	IO_VB4N1_C8	C8
DATA_BUS[251]	IO_VB4N1_C9	C9
DATA_BUS[252]	IO_VB4N1_C10	C10
DATA_BUS[253]	IO_VB4N1_D7	D7
DATA_BUS[254]	IO_VB4N1_D8	D8
DATA_BUS[255]	IO_VB4N1_D9	D9
DATA_BUS[256]	IO_VB4N1_D10	D10
DATA_BUS[257]	IO_VB4N1_E10	E10
DATA_BUS[258]	IO_VB4N1_G13	G13
DATA_BUS[259]	IO_VB4N1_G14	G14
DATA_BUS[260]	IO_VB4N1_G15	G15
DATA_BUS[261]	IO_VB4N1_H13	H13

DATA_BUS[262]	IO_VB4N1_H14	H14
DATA_BUS[263]	IO_VB4N1_J12	J12
DATA_BUS[264]	IO_VB4N1_J13	J13
DATA_BUS[265]	IO_VB4N1_K14	K14
DATA_BUS[266]	IO_VB4N1_L14	L14
DATA_BUS[267]	IO_VB4N1_L15	L15
DATA_BUS[268]	IO_VB4N1_M15	M15
DATA_BUS[269]	IO_VB4N1_M16	M16
DATA_BUS[270]	IO_VB4N1_A6	A6
DATA_BUS[271]	IO_VB4N0_A5	A5
DATA_BUS[272]	IO_VB4N0_B5	B5
DATA_BUS[273]	IO_VB4N0_B6	B6
DATA_BUS[274]	IO_VB4N0_C5	C5
DATA_BUS[275]	IO_VB4N0_C6	C6
DATA_BUS[276]	IO_VB4N0_D6	D6
DATA_BUS[277]	IO_VB4N0_E9	E9
DATA_BUS[278]	IO_VB4N0_F10	F10
DATA_BUS[279]	IO_VB4N0_F11	F11
DATA_BUS[280]	IO_VB4N0_G11	G11
DATA_BUS[281]	IO_VB4N0_G12	G12
DATA_BUS[282]	IO_VB4N0_H11	H11
DATA_BUS[283]	IO_VB4N0_H12	H12
DATA_BUS[284]	IO_VB4N1_A7	A7
DATA_BUS[285]	IO_VB4N1_A8	A8
DATA_BUS[286]	IO_VB4N0_L13	L13
DATA_BUS[287]	IO_VB4N0_M13	M13
DATA_BUS[288]	IO_VB4N0_M14	M14
DATA_BUS[289]	IO_VB4N0_N13	N13
DATA_BUS[290]	IO_VB4N0_N14	N14
DATA_BUS[291]	IO_VB4N0_N15	N15
DATA_BUS[292]	IO_VB4N0_P15	P15
DATA_BUS[293]	RUP4	E8
DATA_BUS[294]	RDN4	J11
DATA_BUS[295]	IO_VB2N3_J38	J38
DATA_BUS[296]	IO_VB2N3_J39	J39
DATA_BUS[297]	IO_VB2N3_K38	K38
DATA_BUS[298]	IO_VB2N3_H38	H38
DATA_BUS[299]	IO_VB2N3_H39	H39
DATA_BUS[300]	IO_VB2N2_J36	J36
DATA_BUS[301]	IO_VB2N2_J37	J37
DATA_BUS[302]	IO_VB2N2_K36	K36
DATA_BUS[303]	IO_VB2N2_K37	K37
DATA_BUS[304]	IO_VB2N2_L34	L34
DATA_BUS[305]	IO_VB2N2_L35	L35
DATA_BUS[306]	IO_VB2N2_L36	L36
DATA_BUS[307]	IO_VB2N2_L37	L37
DATA_BUS[308]	IO_VB2N2_M34	M34
DATA_BUS[309]	IO_VB2N2_M35	M35
DATA_BUS[310]	IO_VB2N2_M36	M36
DATA_BUS[311]	IO_VB2N2_M37	M37
DATA_BUS[312]	IO_VB2N2_N32	N32

DATA_BUS[313]	IO_VB2N2_N33	N33
DATA_BUS[314]	IO_VB2N2_N34	N34
DATA_BUS[315]	IO_VB2N2_N35	N35
DATA_BUS[316]	IO_VB2N2_P26	P26
DATA_BUS[317]	IO_VB2N2_P27	P27
DATA_BUS[318]	IO_VB2N2_P28	P28
DATA_BUS[319]	IO_VB2N2_P29	P29
DATA_BUS[320]	IO_VB2N2_P30	P30
DATA_BUS[321]	IO_VB2N2_P31	P31
DATA_BUS[322]	IO_VB2N2_P32	P32
DATA_BUS[323]	IO_VB2N2_P33	P33
DATA_BUS[324]	IO_VB2N2_R27	R27
DATA_BUS[325]	IO_VB2N2_R28	R28
DATA_BUS[326]	IO_VB2N2_R31	R31
DATA_BUS[327]	IO_VB2N2_R32	R32
DATA_BUS[328]	IO_VB2N2_F38	F38
DATA_BUS[329]	IO_VB2N2_F39	F39
DATA_BUS[330]	IO_VB2N2_G36	G36
DATA_BUS[331]	IO_VB2N2_G37	G37
DATA_BUS[332]	IO_VB2N2_G38	G38
DATA_BUS[333]	IO_VB2N2_G39	G39
DATA_BUS[334]	IO_VB2N2_H36	H36
DATA_BUS[335]	IO_VB2N2_H37	H37
DATA_BUS[336]	IO_VB2N1_B37	B37
DATA_BUS[337]	IO_VB2N1_B38	B38
DATA_BUS[338]	IO_VB2N1_D36	D36
DATA_BUS[339]	IO_VB2N1_D37	D37
DATA_BUS[340]	IO_VB2N1_E34	E34
DATA_BUS[341]	IO_VB2N1_E35	E35
DATA_BUS[342]	IO_VB2N1_E36	E36
DATA_BUS[343]	IO_VB2N1_E37	E37
DATA_BUS[344]	IO_VB2N1_E38	E38
DATA_BUS[345]	IO_VB2N1_E39	E39
DATA_BUS[346]	IO_VB2N1_F34	F34
DATA_BUS[347]	IO_VB2N1_F35	F35
DATA_BUS[348]	IO_VB2N1_F36	F36
DATA_BUS[349]	IO_VB2N1_F37	F37
DATA_BUS[350]	IO_VB2N1_G34	G34
DATA_BUS[351]	IO_VB2N1_G35	G35
DATA_BUS[352]	IO_VB2N1_H31	H31
DATA_BUS[353]	IO_VB2N1_H32	H32
DATA_BUS[354]	IO_VB2N1_H34	H34
DATA_BUS[355]	IO_VB2N1_H35	H35
DATA_BUS[356]	IO_VB2N1_J33	J33
DATA_BUS[357]	IO_VB2N1_J34	J34
DATA_BUS[358]	IO_VB2N1_K31	K31
DATA_BUS[359]	IO_VB2N1_K32	K32
DATA_BUS[360]	IO_VB2N1_K34	K34
DATA_BUS[361]	IO_VB2N1_K35	K35
DATA_BUS[362]	IO_VB2N1_L32	L32
DATA_BUS[363]	IO_VB2N1_L33	L33

DATA_BUS[364]	IO_VB2N1_M30	M30
DATA_BUS[365]	IO_VB2N1_M31	M31
DATA_BUS[366]	IO_VB2N1_M32	M32
DATA_BUS[367]	IO_VB2N1_M33	M33
DATA_BUS[368]	IO_VB2N1_N28	N28
DATA_BUS[369]	IO_VB2N1_N29	N29
DATA_BUS[370]	IO_VB2N1_N30	N30
DATA_BUS[371]	IO_VB2N1_N31	N31
DATA_BUS[372]	IO_VB2N0_C36	C36
DATA_BUS[373]	IO_VB2N0_C37	C37
DATA_BUS[374]	IO_VB2N0_J31	J31
DATA_BUS[375]	IO_VB2N0_J32	J32
DATA_BUS[376]	IO_VB2N0_L30	L30
DATA_BUS[377]	IO_VB2N0_L31	L31
DATA_BUS[378]	IO_VB7N0_AH20	AH20
DATA_BUS[379]	IO_VB7N0_AL18	AL18
DATA_BUS[380]	IO_VB7N0_AM18	AM18
DATA_BUS[381]	IO_VB7N0_AM19	AM19
DATA_BUS[382]	IO_VB7N0_AN18	AN18
DATA_BUS[383]	IO_VB7N0_AN19	AN19
DATA_BUS[384]	IO_VB7N0_AP16	AP16
DATA_BUS[385]	IO_VB7N0_AP19	AP19
DATA_BUS[386]	IO_VB7N0_AR16	AR16
DATA_BUS[387]	IO_VB7N0_AR20	AR20
DATA_BUS[388]	IO_VB7N0_AT16	AT16
DATA_BUS[389]	IO_VB7N0_AT17	AT17
DATA_BUS[390]	IO_VB7N0_AU17	AU17
DATA_BUS[391]	IO_VB7N0_AV16	AV16
DATA_BUS[392]	IO_VB7N0_AV17	AV17
DATA_BUS[393]	IO_VB7N0_AW17	AW17
DATA_BUS[394]	IO_VB7N1_AG19	AG19
DATA_BUS[395]	IO_VB7N1_AG20	AG20
DATA_BUS[396]	IO_VB7N1_AH19	AH19
DATA_BUS[397]	IO_VB7N1_AJ18	AJ18
DATA_BUS[398]	IO_VB7N1_AK17	AK17
DATA_BUS[399]	IO_VB7N1_AL16	AL16
DATA_BUS[400]	IO_VB7N1_AL17	AL17
DATA_BUS[401]	IO_VB7N1_AM17	AM17
DATA_BUS[402]	IO_VB7N1_AN17	AN17
DATA_BUS[403]	IO_VB7N1_AP14	AP14
DATA_BUS[404]	IO_VB7N1_AP18	AP18
DATA_BUS[405]	IO_VB7N1_AR14	AR14
DATA_BUS[406]	IO_VB7N1_AR15	AR15
DATA_BUS[407]	IO_VB7N1_AT13	AT13
DATA_BUS[408]	IO_VB7N1_AT14	AT14
DATA_BUS[409]	IO_VB7N1_AT15	AT15
DATA_BUS[410]	IO_VB7N1_AU13	AU13
DATA_BUS[411]	IO_VB7N1_AU14	AU14
DATA_BUS[412]	IO_VB7N1_AU15	AU15
DATA_BUS[413]	IO_VB7N1_AU16	AU16
DATA_BUS[414]	IO_VB7N1_AV13	AV13

DATA_BUS[415]	IO_VB7N1_AV14	AV14
DATA_BUS[416]	IO_VB7N1_AV15	AV15
DATA_BUS[417]	IO_VB7N1_AW13	AW13
DATA_BUS[418]	IO_VB7N1_AW14	AW14
DATA_BUS[419]	IO_VB7N1_AW15	AW15
DATA_BUS[420]	IO_VB7N2_AG17	AG17
DATA_BUS[421]	IO_VB7N2_AG18	AG18
DATA_BUS[422]	IO_VB7N2_AH17	AH17
DATA_BUS[423]	IO_VB7N2_AH18	AH18
DATA_BUS[424]	IO_VB7N2_AJ16	AJ16
DATA_BUS[425]	IO_VB7N2_AJ17	AJ17
DATA_BUS[426]	IO_VB7N2_AK15	AK15
DATA_BUS[427]	IO_VB7N2_AK16	AK16
DATA_BUS[428]	IO_VB7N2_AL14	AL14
DATA_BUS[429]	IO_VB7N2_AL15	AL15
DATA_BUS[430]	IO_VB7N2_AM15	AM15
DATA_BUS[431]	IO_VB7N2_AM16	AM16
DATA_BUS[432]	IO_VB7N2_AN15	AN15
DATA_BUS[433]	IO_VB7N2_AN16	AN16
DATA_BUS[434]	IO_VB7N2_AP13	AP13
DATA_BUS[435]	IO_VB7N2_AR11	AR11
DATA_BUS[436]	IO_VB7N2_AR12	AR12
DATA_BUS[437]	IO_VB7N2_AR13	AR13
DATA_BUS[438]	IO_VB7N2_AT11	AT11
DATA_BUS[439]	IO_VB7N2_AT12	AT12
DATA_BUS[440]	IO_VB7N2_AU11	AU11
DATA_BUS[441]	IO_VB7N2_AU12	AU12
DATA_BUS[442]	IO_VB7N2_AV10	AV10
DATA_BUS[443]	IO_VB7N2_AV11	AV11
DATA_BUS[444]	IO_VB7N2_AV12	AV12
DATA_BUS[445]	IO_VB7N2_AW10	AW10
DATA_BUS[446]	IO_VB7N2_AW11	AW11
DATA_BUS[447]	IO_VB7N2_AW12	AW12
DATA_BUS[448]	IO_VB7N3_AG15	AG15
DATA_BUS[449]	IO_VB7N3_AG16	AG16
DATA_BUS[450]	IO_VB7N3_AH14	AH14
DATA_BUS[451]	IO_VB7N3_AH15	AH15
DATA_BUS[452]	IO_VB7N3_AH16	AH16
DATA_BUS[453]	IO_VB7N3_AJ14	AJ14
DATA_BUS[454]	IO_VB7N3_AJ15	AJ15
DATA_BUS[455]	IO_VB7N3_AK13	AK13
DATA_BUS[456]	IO_VB7N3_AK14	AK14
DATA_BUS[457]	IO_VB7N3_AL13	AL13
DATA_BUS[458]	IO_VB7N3_AM13	AM13
DATA_BUS[459]	IO_VB7N3_AM14	AM14
DATA_BUS[460]	IO_VB7N3_AN14	AN14
DATA_BUS[461]	IO_VB7N3_AR9	AR9
DATA_BUS[462]	IO_VB7N3_AR10	AR10
DATA_BUS[463]	IO_VB7N3_AT7	AT7
DATA_BUS[464]	IO_VB7N3_AT8	AT8
DATA_BUS[465]	IO_VB7N3_AT9	AT9

DATA_BUS[466]	IO_VB7N3_AT10	AT10
DATA_BUS[467]	IO_VB7N3_AU7	AU7
DATA_BUS[468]	IO_VB7N3_AU8	AU8
DATA_BUS[469]	IO_VB7N3_AU9	AU9
DATA_BUS[470]	IO_VB7N3_AU10	AU10
DATA_BUS[471]	IO_VB7N3_AV7	AV7
DATA_BUS[472]	IO_VB7N3_AV8	AV8
DATA_BUS[473]	IO_VB7N3_AV9	AV9
DATA_BUS[474]	IO_VB7N3_AW7	AW7
DATA_BUS[475]	IO_VB7N3_AW8	AW8
DATA_BUS[476]	IO_VB7N3_AW9	AW9
DATA_BUS[477]	IO_VB7N4_AG14	AG14
DATA_BUS[478]	IO_VB7N4_AH13	AH13
DATA_BUS[479]	IO_VB7N4_AJ12	AJ12
DATA_BUS[480]	IO_VB7N4_AJ13	AJ13
DATA_BUS[481]	IO_VB7N4_AK12	AK12
DATA_BUS[482]	IO_VB7N4_AL12	AL12
DATA_BUS[483]	IO_VB7N4_AM11	AM11
DATA_BUS[484]	IO_VB7N4_AM12	AM12
DATA_BUS[485]	IO_VB7N4_AN11	AN11
DATA_BUS[486]	IO_VB7N4_AN12	AN12
DATA_BUS[487]	IO_VB7N4_AN13	AN13
DATA_BUS[488]	IO_VB7N4_AP8	AP8
DATA_BUS[489]	IO_VB7N4_AP10	AP10
DATA_BUS[490]	IO_VB7N4_AP11	AP11
DATA_BUS[491]	IO_VB7N4_AR8	AR8
DATA_BUS[492]	IO_VB7N4_AU5	AU5
DATA_BUS[493]	IO_VB7N4_AU6	AU6
DATA_BUS[494]	IO_VB7N4_AV5	AV5
DATA_BUS[495]	IO_VB7N4_AV6	AV6
DATA_BUS[496]	IO_VB7N4_AW5	AW5
DATA_BUS[497]	IO_VB7N4_AW6	AW6
DATA_BUS[498]	RDN7	AL11
DATA_BUS[499]	RUP7	AN9
DATA_BUS[500]	IO_VB8N4_AT24	AT24
DATA_BUS[501]	IO_VB8N4_AU23	AU23
DATA_BUS[502]	CLK13n	D19
DATA_BUS[503]	CLK13p	C19
DATA_BUS[504]	CLK14n	D21
DATA_BUS[505]	CLK14p	C21
DATA_BUS[506]	PLL6_FBn	AR18
DATA_BUS[507]	PLL6_FBp	AT18
DATA_BUS[508]	PLL6_OUT0n	AV19
DATA_BUS[509]	PLL6_OUT0p	AW19
DATA_BUS[510]	PLL6_OUT1n	AU18
DATA_BUS[511]	PLL6_OUT1p	AV18

Table 7.1: 512-bit bus connection to the *DUT-FPGA#1*.

The signal *DATA_BUS[503]* is connected to the clock input pin 13. The signal *DATA_BUS[505]* is connected to the clock input pin 14. The signals *DATA_BUS[507]*, *DATA_BUS[509]* and *DATA_BUS[511]* are connected to the PLL output pins of PLL 5.

7.2.1 LVDS connection to DUT-FPGA#1

Differential Receive Channels

The signals in table 7.2 show the receiver pairs for the LVDS connection to the *DUT-FPGA#2*.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
RX1_TX2-[0]	CLK8n	Y2
RX1_TX2-[1]	IO_VB6N4_AA2	AA2
RX1_TX2-[2]	IO_VB6N4_AA4	AA4
RX1_TX2-[3]	IO_VB6N4_AB3	AB3
RX1_TX2-[4]	IO_VB6N4_AC2	AC2
RX1_TX2-[5]	IO_VB6N4_AB5	AB5
RX1_TX2-[6]	IO_VB6N4_AE2	AE2
RX1_TX2-[7]	IO_VB6N4_AD3	AD3
RX1_TX2-[8]	IO_VB6N3_AC4	AC4
RX1_TX2-[9]	IO_VB6N3_AE4	AE4
RX1_TX2-[10]	IO_VB6N3_AD5	AD5
RX1_TX2-[11]	IO_VB6N3_AF2	AF2
RX1_TX2-[12]	IO_VB6N3_AG2	AG2
RX1_TX2-[13]	IO_VB6N3_AH2	AH2
RX1_TX2-[14]	IO_VB6N3_AF4	AF4
RX1_TX2-[15]	IO_VB6N3_AJ2	AJ2
RX1_TX2-[16]	CLK10n	W2
RX1_TX2-[17]	IO_VB5N0_U2	U2
RX1_TX2-[18]	IO_VB5N0_V3	V3
RX1_TX2-[19]	IO_VB5N0_R2	R2
RX1_TX2-[20]	IO_VB5N0_T3	T3
RX1_TX2-[21]	IO_VB5N0_V5	V5
RX1_TX2-[22]	IO_VB5N0_U4	U4
RX1_TX2-[23]	IO_VB5N0_P2	P2
RX1_TX2-[24]	IO_VB5N0_P4	P4
RX1_TX2-[25]	IO_VB5N1_R4	R4
RX1_TX2-[26]	IO_VB5N1_T5	T5
RX1_TX2-[27]	IO_VB5N1_N2	N2
RX1_TX2-[28]	IO_VB5N1_M2	M2
RX1_TX2-[29]	IO_VB5N1_L2	L2
RX1_TX2-[30]	IO_VB5N1_K2	K2
RX1_TX2-[31]	IO_VB5N1_N4	N4
RX1_TX2+[0]	CLK8p	Y1
RX1_TX2+[1]	IO_VB6N4_AA1	AA1
RX1_TX2+[2]	IO_VB6N4_AA3	AA3
RX1_TX2+[3]	IO_VB6N4_AB2	AB2
RX1_TX2+[4]	IO_VB6N4_AC1	AC1
RX1_TX2+[5]	IO_VB6N4_AB4	AB4
RX1_TX2+[6]	IO_VB6N4_AE1	AE1
RX1_TX2+[7]	IO_VB6N4_AD2	AD2
RX1_TX2+[8]	IO_VB6N3_AC3	AC3
RX1_TX2+[9]	IO_VB6N3_AE3	AE3

RX1_TX2+[10]	IO_VB6N3_AD4	AD4
RX1_TX2+[11]	IO_VB6N3_AF1	AF1
RX1_TX2+[12]	IO_VB6N3_AG1	AG1
RX1_TX2+[13]	IO_VB6N3_AH1	AH1
RX1_TX2+[14]	IO_VB6N3_AF3	AF3
RX1_TX2+[15]	IO_VB6N3_AJ1	AJ1
RX1_TX2+[16]	CLK10p	W1
RX1_TX2+[17]	IO_VB5N0_U1	U1
RX1_TX2+[18]	IO_VB5N0_V2	V2
RX1_TX2+[19]	IO_VB5N0_R1	R1
RX1_TX2+[20]	IO_VB5N0_T2	T2
RX1_TX2+[21]	IO_VB5N0_V4	V4
RX1_TX2+[22]	IO_VB5N0_U3	U3
RX1_TX2+[23]	IO_VB5N0_P1	P1
RX1_TX2+[24]	IO_VB5N0_P3	P3
RX1_TX2+[25]	IO_VB5N1_R3	R3
RX1_TX2+[26]	IO_VB5N1_T4	T4
RX1_TX2+[27]	IO_VB5N1_N1	N1
RX1_TX2+[28]	IO_VB5N1_M1	M1
RX1_TX2+[29]	IO_VB5N1_L1	L1
RX1_TX2+[30]	IO_VB5N1_K1	K1
RX1_TX2+[31]	IO_VB5N1_N3	N3

Table 7.2: LVDS connection to the *DUT-FPGA#1*: Receive channels.

The differential signals *RX1_TX2[0]* are connected to the differential clock input pins 2. The differential signals *RX1_TX2[16]* are connected to the differential clock input pins 0.

Differential Transmit Channels

The signals in table 7.3 show the transmitter pairs for the LVDS connection to the *DUT-FPGA#2*.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
TX1_RX2-[0]	IO_VB6N4_Y14	Y14
TX1_RX2-[1]	IO_VB6N4_AA12	AA12
TX1_RX2-[2]	IO_VB6N4_AA10	AA10
TX1_RX2-[3]	IO_VB6N4_Y8	Y8
TX1_RX2-[4]	IO_VB6N4_Y6	Y6
TX1_RX2-[5]	IO_VB6N4_AA14	AA14
TX1_RX2-[6]	IO_VB6N4_AB11	AB11
TX1_RX2-[7]	IO_VB6N3_AA8	AA8
TX1_RX2-[8]	IO_VB6N3_AB9	AB9
TX1_RX2-[9]	IO_VB6N3_AB7	AB7
TX1_RX2-[10]	IO_VB6N3_AB13	AB13
TX1_RX2-[11]	IO_VB6N3_AC11	AC11
TX1_RX2-[12]	IO_VB6N3_AC9	AC9
TX1_RX2-[13]	IO_VB6N3_AC13	AC13
TX1_RX2-[14]	IO_VB6N3_AC7	AC7
TX1_RX2-[15]	IO_VB6N3_AD9	AD9
TX1_RX2-[16]	IO_VB5N0_W8	W8

TX1_RX2-[17]	IO_VB5N0_W13	W13
TX1_RX2-[18]	IO_VB5N0_V7	V7
TX1_RX2-[19]	IO_VB5N0_V9	V9
TX1_RX2-[20]	IO_VB5N0_V13	V13
TX1_RX2-[21]	IO_VB5N0_U13	U13
TX1_RX2-[22]	IO_VB5N0_U11	U11
TX1_RX2-[23]	IO_VB5N0_U7	U7
TX1_RX2-[24]	IO_VB5N1_U9	U9
TX1_RX2-[25]	IO_VB5N1_T7	T7
TX1_RX2-[26]	IO_VB5N1_T13	T13
TX1_RX2-[27]	IO_VB5N1_T11	T11
TX1_RX2-[28]	IO_VB5N1_T9	T9
TX1_RX2-[29]	IO_VB5N1_R7	R7
TX1_RX2-[30]	IO_VB5N1_P6	P6
TX1_RX2-[31]	IO_VB5N1_R13	R13
TX1_RX2+[0]	IO_VB6N4_Y13	Y13
TX1_RX2+[1]	IO_VB6N4_AA11	AA11
TX1_RX2+[2]	IO_VB6N4_AA9	AA9
TX1_RX2+[3]	IO_VB6N4_Y7	Y7
TX1_RX2+[4]	IO_VB6N4_Y5	Y5
TX1_RX2+[5]	IO_VB6N4_AA13	AA13
TX1_RX2+[6]	IO_VB6N4_AB10	AB10
TX1_RX2+[7]	IO_VB6N3_AA7	AA7
TX1_RX2+[8]	IO_VB6N3_AB8	AB8
TX1_RX2+[9]	IO_VB6N3_AB6	AB6
TX1_RX2+[10]	IO_VB6N3_AB12	AB12
TX1_RX2+[11]	IO_VB6N3_AC10	AC10
TX1_RX2+[12]	IO_VB6N3_AC8	AC8
TX1_RX2+[13]	IO_VB6N3_AC12	AC12
TX1_RX2+[14]	IO_VB6N3_AC6	AC6
TX1_RX2+[15]	IO_VB6N3_AD8	AD8
TX1_RX2+[16]	IO_VB5N0_W7	W7
TX1_RX2+[17]	IO_VB5N0_W12	W12
TX1_RX2+[18]	IO_VB5N0_V6	V6
TX1_RX2+[19]	IO_VB5N0_V8	V8
TX1_RX2+[20]	IO_VB5N0_V12	V12
TX1_RX2+[21]	IO_VB5N0_U12	U12
TX1_RX2+[22]	IO_VB5N0_U10	U10
TX1_RX2+[23]	IO_VB5N0_U6	U6
TX1_RX2+[24]	IO_VB5N1_U8	U8
TX1_RX2+[25]	IO_VB5N1_T6	T6
TX1_RX2+[26]	IO_VB5N1_T12	T12
TX1_RX2+[27]	IO_VB5N1_T10	T10
TX1_RX2+[28]	IO_VB5N1_T8	T8
TX1_RX2+[29]	IO_VB5N1_R6	R6
TX1_RX2+[30]	IO_VB5N1_P5	P5
TX1_RX2+[31]	IO_VB5N1_R12	R12

Table 7.3: LVDS connection to the *DUT-FPGA#1*: Transmit channels.

7.3 Connection to the CPLD for Clock Factory and Configuration

7.3.1 Configuration Pins for the DUT-FPGA#1 by the CPLD for Clock Factory and Configuration

The signals in table 7.4 can also be reached by the *Hpe_childboard* 1. Only the signals *CB1_DATA[0]* to *CB1_DATA[7]* can be used as normal I/O pins. The others are only for configuration (refer to section 3.2).

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
CB1_CONFIG#	nCONFIG	AM30
CB1_CONF_DONE	CONF_DONE	F33
CB1_DATA[0]	DATA0	H22
CB1_DATA[1]	DATA1	F21
CB1_DATA[2]	DATA2	E31
CB1_DATA[3]	DATA3	E33
CB1_DATA[4]	DATA4	H29
CB1_DATA[5]	DATA5	J29
CB1_DATA[6]	DATA6	E32
CB1_DATA[7]	DATA7	F32
CB1_DCLK	DCLK	D34
CB1_STATUS#	nSTATUS	A37

Table 7.4: Pin connection to the *Hpe_childboard* 1 connector: Configuration pins for the two DUT-FPGAs.

7.3.2 Clocks

The signals in table 7.5 are input clocks driven by the *Clock Factory*. For further details see section 3.1.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
DUT1_CLK3P	CLK3p	Y37
DUT1_CLK6P	CLK6p	AW20
DUT1_CLK7-	CLK7n	AT19
DUT1_CLK7+	CLK7p	AU19
DUT1_CLK9P	CLK9p	Y3
DUT1_CLK12P	CLK12p	A20
DUT1_CLK15-	CLK15n	D20
DUT1_CLK15+	CLK15p	C20

Table 7.5: Clocks from the *Clock Factory*.

The differential clocks *DUT1_CLK7** and *DUT1_CLK15** are delivered in *LVPECL* standard. The pins *DUT1_CLK7-* and *DUT1_CLK15-* are not connected to the *Clock Factory* but only used for the inverted clock signal. All other clocks are driven in normal single ended standard.

7.3.3 I/O Pins: Negative Clock Inputs

The signals in table 7.6 are the negative clock input pins. Since the *Clock Factory* is not able to drive differential clocks, these pins can be used as normal I/O pins between the *DUT-FPGA#1* and the *Clock Factory*.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
DUT1_CLK1N	CLK1n	W36
DUT1_CLK3N	CLK3n	Y36
DUT1_CLK5N	CLK5n	AT21
DUT1_CLK6N	CLK6n	AV20
DUT1_CLK9N	CLK9n	Y4
DUT1_CLK11N	CLK11n	W4
DUT1_CLK12N	CLK12n	B20

Table 7.6: Negative clock inputs from *Clock Factory*. This signals can be used as normal I/O pins.

7.3.4 Fast PLL Clock Inputs

The signals that end with a *P* in table 7.7 are single ended clock input pins for driving the Fast PLLs in the *DUT-FPGA#1*. Since the *Clock Factory* is not able to drive differential clocks, the pins that end with an *N* can be used as normal I/O pins between the *DUT-FPGA#1* and the *Clock Factory*.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
DUT1_FPLL7N	FPLL7CLKn	C38
DUT1_FPLL7P	FPLL7CLKp	C39
DUT1_FPLL8N	FPLL8CLKn	AU38
DUT1_FPLL8P	FPLL8CLKp	AU39
DUT1_FPLL9N	FPLL9CLKn	AU2
DUT1_FPLL9P	FPLL9CLKp	AU1
DUT1_FPLL10N	FPLL10CLKn	C2
DUT1_FPLL10P	FPLL10CLKp	C1

Table 7.7: Fast PLL clock inputs. The negative clock inputs can be used as normal I/O pins.

7.3.5 PLL Output Clocks

The signals that end with a *P* in table 7.8 are output clocks which are sent to the *Clock Factory* from where they can be distributed to all input clocks connected to the *Clock Factory*. Although the negative pins (end with an *N*) are connected, they can not be used since the *Clock Factory* is not able to receive differential clocks.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
DUT1_PLL12O1N	PLL12_OUT1n	AU22
DUT1_PLL12O1P	PLL12_OUT1p	AV22

Table 7.8: PLL output clocks. The negative clock outputs can be used as normal I/O pins.

7.3.6 Other I/O pins

Table 7.9 gives you all other signals connected between *DUT-FPGA#1* and *Clock Factory*.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
DUT1_CLKUSR	CLKUSR	AP30
DUT1_CRC_ERROR	CRC_ERROR	G22
DUT1_CS	CS	AR32
DUT1_CS#	nCS	AP21
DUT1_DEV_OE	DEV_OE	AN20
DUT1_RDY#_BSY	RDYnBSY	G31
DUT1_RS#	nRS	AR30
DUT1_RU#_LU	RUnLU	AM20
DUT1_WS#	nWS	AR31

Table 7.9: All other I/O pins between *DUT-FPGA#1* and *Clock Factory*.

7.4 Connection to the CPLD for USB Blaster and FCP

The signals in table 7.10 are internal signals needed for maintenance. Please do not use them.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
DUT1_INIT_DONE	INIT_DONE	H30
DUT1_PGM[0]	PGM0	G21
DUT1_PGM[1]	PGM1	F20
DUT1_PGM[2]	PGM2	E20

Table 7.10: Pins needed for the FCP.

7.5 Dedicated Pins on the DUT-FPGA#1

7.5.1 Thermal Control

The signals in table 7.11 can not be used as I/O pins. They are needed for the thermal control of the *DUT-FPGA#1*. For more information refer to section 3.3.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
DUT1_TEMPDIODE-	TEMPDIODEn	F7
DUT1_TEMPDIODE+	TEMPDIODEp	B4

Table 7.11: Temperature diode.

7.5.2 JTAG Pins

The signals in table 7.12 are dedicated JTAG pins. They can not be used as I/O pins.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
DUT1_TDI	TDI	AN31
DUT1_TDO	TDO	F8
TCK_DUT	TCK	AP32
TMS_DUT	TMS	AP33
MIDI_TRST	TRST	AW37

Table 7.12: JTAG signals.

7.5.3 Configuration Pins

The signals in table 7.13 can be reached by the *Hpe_childboard* 1 and by the *Clock Factory*. Only the signals *CB1_DATA[0]* to *CB1_DATA[7]* can be used as normal I/O pins, the others are only for configuration. For configuration refer to section 3.2.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
CB1_CONFIG#	nCONFIG	AM30
CB1_CONF_DONE	CONF_DONE	F33
CB1_DATA[0]	DATA0	H22
CB1_DATA[1]	DATA1	F21
CB1_DATA[2]	DATA2	E31
CB1_DATA[3]	DATA3	E33
CB1_DATA[4]	DATA4	H29
CB1_DATA[5]	DATA5	J29
CB1_DATA[6]	DATA6	E32
CB1_DATA[7]	DATA7	F32
CB1_DCLK	DCLK	D34
CB1_STATUS#	nSTATUS	A37

Table 7.13: Pin connection to the *Hpe_childboard* 1 connector: Configuration pins for the *DUT-FPGA#1*.

7.5.4 Other dedicated Configuration Pins

The signals in table 7.14 are other dedicated configuration pins. They can not be used as I/O pins.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
D1_CEO#_D2_CE#	nCEO	AT6
DUT1_IO_PULLUP#	nIO_PULLUP	AT5
DUT1_MSEL[0]	MSEL0	H10
DUT1_MSEL[1]	MSEL1	G9
DUT1_MSEL[2]	MSEL2	E7
DUT1_MSEL[3]	MSEL3	A3
DUT1_PORSEL	PORSEL	AP7

Table 7.14: Dedicated configuration pins.

- *D1_CEO#_D2_CE#:* Dedicated pin, that ensures that *DUT-FPGA#1* is configured before *DUT-FPGA#2*.
- *DUT1_IO_PULLUP:* Dedicated pin that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins are on or off before and during configuration. These pull-ups are turned on by default.
- *DUT1_MSEL:* Configuration input pins that set the *Altera Stratix II* device configuration scheme. Set to *Fast Passive Parallel* mode by default.
- *DUT1_PORSEL:* Dedicated pin, that selects between a *Power On Reset* time of 12 ms or 100 ms. Set to 12 ms by default.

For further details of these pins refer to the handbook of the *Altera Stratix II*.

7.6 JTAG Pins for internal JTAG Core

The signals in table 7.15 are normal I/O signals that can be set into the JTAG chain (refer to section 4.2 for further details) if a JTAG core is developed with the *HMX2-AS2*.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
TCK_INT	IO_VB8N4_AU24	AU24
TDI_INT1	IO_VB8N4_AV24	AV24
TDOI_INT1_INT2	IO_VB8N4_AW23	AW23
TMS_INT	IO_VB8N4_AV23	AV23

Table 7.15:
These pins can be switched into the JTAG chain of the *HMX2-AS2* via the *Communication Controller* on the *HC-PCIe*.

7.7 Clock from Oscillator

The 100 MHz clock in table 7.16 is needed for the LVDS connection between the *HMX2-AS2* and the *Communication Controller* on the *HC-PCIe* (which has to be connected to the *Hpe_childboard* 1 connector for *SEmulation* mode).

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
DUT1_CLK100M[1]	CLK11p	W3
DUT1_CLK100M[2]	CLK1p	W37

Table 7.16: 100 MHz clock from an external oscillator.

7.8 Hpe_Childboard 1

Only on the *Hpe_childboard* 1 connector the *SEmulator Hpe_childboard* can be connected.

In order to be able to use LVDS signalling the *DUT-FPGA#1* requires an I/O supply of 2.5 V on the banks involved. By default these 2.5 V are provided. They are necessary when a *Hpe_childboard* with differential signals is connected to the connector X3. However, when a *Hpe_childboard* without any LVDS signals is connected to X3, then the I/O supply of the concerned banks can be changed to 3.3 V. A low on the signal *CB1_SEL_LVDS_VAL*, controlled by the *Hpe_childboard* 1 switches to 3.3 V. By default this signal is set to high by a pull-up resistor, hence 2.5 V are provided.

For a description of the pins, refer to 5.2.1. All I/O pins of this *Hpe_childboard* that are not connected to the *DUT-FPGA#1*, are connected to *DUT-FPGA#2*.

7.8.1 Differential Receive Channels

The signals in table 7.17 are the differential receiver channels from the *Hpe_childboard* 1.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*	*Childboard connector pin*
CB1_RX_CLK1+	CLK0p	W39	A2
CB1_RX_CLK1-	CLK0n	W38	A4
CB1_RX+[01]	IO_VB2N4_U39	U39	A6
CB1_RX-[01]	IO_VB2N4_U38	U38	A8
CB1_RX+[02]	IO_VB2N4_V38	V38	A10
CB1_RX-[02]	IO_VB2N4_V37	V37	A12
CB1_RX+[03]	IO_VB2N4_R39	R39	A14
CB1_RX-[03]	IO_VB2N4_R38	R38	A16
CB1_RX_CLK3+	IO_VB2N4_T38	T38	B2
CB1_RX_CLK3-	IO_VB2N4_T37	T37	B4
CB1_RX+[07]	IO_VB2N4_V36	V36	B6
CB1_RX-[07]	IO_VB2N4_V35	V35	B8
CB1_RX+[08]	IO_VB2N4_U37	U37	B10
CB1_RX-[08]	IO_VB2N4_U36	U36	B12
CB1_RX+[09]	IO_VB2N4_P39	P39	B14
CB1_RX-[09]	IO_VB2N4_P38	P38	B16
CB1_RX_CLK4+	IO_VB2N4_P37	P37	B18
CB1_RX_CLK4-	IO_VB2N4_P36	P36	B20
CB1_RX+[10]	IO_VB2N3_R37	R37	B22
CB1_RX-[10]	IO_VB2N3_R36	R36	B24
CB1_RX+[11]	IO_VB2N3_T36	T36	B26
CB1_RX-[11]	IO_VB2N3_T35	T35	B28
CB1_RX+[12]	IO_VB2N3_N39	N39	B30
CB1_RX-[12]	IO_VB2N3_N38	N38	B32

Table 7.17: Pin connection to the *Hpe_childboard* 1 connector: Receive channels.

The differential signals *CB1_RX_CLK1* are connected to the differential clock input pins 10.

7.8.2 Transmit Channels

The signals in table 7.18 are the differential transmitter channels from the *Hpe_childboard* 1.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*	*Childboard connector pin*
CB1_TX_CLK1+	IO_VB2N4_Y27	Y27	A2
CB1_TX_CLK1-	IO_VB2N4_Y26	Y26	A4
CB1_TX+[01]	IO_VB2N4_W28	W28	A6
CB1_TX-[01]	IO_VB2N4_W27	W27	A8
CB1_TX+[02]	IO_VB2N4_W33	W33	A10
CB1_TX-[02]	IO_VB2N4_W32	W32	A12
CB1_TX+[03]	IO_VB2N4_V34	V34	A14
CB1_TX-[03]	IO_VB2N4_V33	V33	A16
CB1_TX_CLK3+	IO_VB2N4_V32	V32	B2
CB1_TX_CLK3-	IO_VB2N4_V31	V31	B4
CB1_TX+[07]	IO_VB2N4_V28	V28	B6
CB1_TX-[07]	IO_VB2N4_V27	V27	B8
CB1_TX+[08]	IO_VB2N4_U28	U28	B10
CB1_TX-[08]	IO_VB2N4_U27	U27	B12
CB1_TX+[09]	IO_VB2N4_U34	U34	B14
CB1_TX-[09]	IO_VB2N4_U33	U33	B16
CB1_TX_CLK4+	IO_VB2N3_U30	U30	B18
CB1_TX_CLK4-	IO_VB2N3_U29	U29	B20
CB1_TX+[10]	IO_VB2N3_U32	U32	B22
CB1_TX-[10]	IO_VB2N3_U31	U31	B24
CB1_TX+[11]	IO_VB2N3_T28	T28	B26
CB1_TX-[11]	IO_VB2N3_T27	T27	B28
CB1_TX+[12]	IO_VB2N3_T34	T34	B30
CB1_TX-[12]	IO_VB2N3_T33	T33	B32

Table 7.18: Pin connection to the *Hpe_childboard* 1 connector: Transmit channels

7.8.3 Configuration Pins for the DUT-FPGA#1 by the Hpe_Childboard 1

The signals in table 7.19 can also be reached by the *Clock Factory*. Only the signals *CB1_DATA[0]* to *CB1_DATA[7]* can be used as normal I/O pins. The others are only for configuration.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*	*Childboard connector pin*
CB1_CONFIG#	nCONFIG	AM30	A62
CB1_CONF_DONE	CONF_DONE	F33	A56
CB1_DATA[0]	DATA0	H22	A53
CB1_DATA[1]	DATA1	F21	A55
CB1_DATA[2]	DATA2	E31	A57
CB1_DATA[3]	DATA3	E33	A59
CB1_DATA[4]	DATA4	H29	A61
CB1_DATA[5]	DATA5	J29	A63
CB1_DATA[6]	DATA6	E32	A65
CB1_DATA[7]	DATA7	F32	A54
CB1_DCLK	DCLK	D34	A60
CB1_STATUS#	nSTATUS	A37	A58

Table 7.19: Pin connection to the *Hpe_childboard* 1 connector: Configuration pins for the two DUT-FPGAs.

7.8.4 Other pins to DUT#1

Table 7.20 gives you an overview of all other signals connected to the *Hpe_childboard* 1.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*	*Childboard connector pin*
CB1_CLK+	PLL12_OUT0p	AW21	A49
CB1_CLK-	PLL12_OUT0n	AV21	A50
CB1_TEST[0]	IO_VB2N3_K39	K39	B56
CB1_TEST[1]	IO_VB2N3_N36	N36	B57
CB1_TEST[2]	IO_VB2N3_N37	N37	B58
CB1_TEST[3]	IO_VB2N3_P34	P34	B59
CB1_EN_TEST#[0]	IO_VB2N3_P35	P35	B60
CB1_EN_TEST#[1]	IO_VB2N3_R29	R29	B61
CB1_EN_TEST#[2]	IO_VB2N3_R30	R30	B62
CB1_EN_TEST#[3]	IO_VB2N3_T29	T29	B63
CB1_RFU[0]	IO_VB2N3_T30	T30	B64
CB1_RFU[1]	IO_VB2N3_T31	T31	B65

Table 7.20: Pin connection to the *Hpe_childboard* 1 connector: Other pins

The differential signals *CB1_CLK** are connected to PLL output pins of the PLL 12.

It is possible to measure 'Z' on 128 signals between *DUT-FPGA#1* and *DUT-FPGA#2*. The signals are *DATA_BUS374* to *DATA_BUS501*. Each of the signals *CB1_EN_TEST#[*]* is an enable for 32 signals on which 'Z' measurement can be performed. Each of the signals *CB1_TEST[*]* initiates the 'Z' measurement for 32 signals. That is to say, the *CB1_TEST[*]* signals pull the bus signals *DATA_BUS374* to *DATA_BUS501* high or low, when *CB1_EN_TEST#[*]* is pulled high.

The signal *CB1_RFU[1]* works as a reset for the differential transceiver.

7.9 Hpe_Childboard 2

Table 7.21 lists all signals connected to this *Hpe_childboard*.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*	*Childboard connector pin*
CB2_BUS[0]	IO_VB3N0_B23	B23	A1
CB2_BUS[1]	IO_VB3N0_C23	C23	A2
CB2_BUS[2]	IO_VB3N0_C24	C24	A3
CB2_BUS[3]	IO_VB3N0_D24	D24	A4
CB2_BUS[4]	IO_VB3N1_D25	D25	A5
CB2_BUS[5]	IO_VB3N1_A25	A25	A6
CB2_BUS[6]	IO_VB3N1_C26	C26	A7
CB2_BUS[7]	IO_VB3N1_C27	C27	A8
CB2_BUS[8]	IO_VB3N1_D26	D26	A9
CB2_BUS[9]	IO_VB3N1_D27	D27	A10
CB2_BUS[10]	IO_VB3N2_A28	A28	A11
CB2_BUS[11]	IO_VB3N2_A29	A29	A12
CB2_BUS[12]	IO_VB3N2_C29	C29	A13
CB2_BUS[13]	IO_VB3N2_C30	C30	A14
CB2_BUS[14]	IO_VB3N2_D29	D29	A15
CB2_BUS[15]	IO_VB3N2_D30	D30	A16

CB2_BUS[16]	IO_VB3N3_A32	A32	A17
CB2_BUS[17]	IO_VB3N3_A31	A31	A18
CB2_BUS[18]	IO_VB3N3_C32	C32	A19
CB2_BUS[19]	IO_VB3N3_C33	C33	A20
CB2_BUS[20]	IO_VB3N3_D32	D32	A21
CB2_BUS[21]	IO_VB3N3_D33	D33	A22
CB2_BUS[22]	IO_VB3N4_A34	A34	A23
CB2_BUS[23]	IO_VB3N4_A35	A35	A24
CB2_BUS[24]	IO_VB3N0_J22	J22	A25
CB2_BUS[25]	IO_VB3N0_M21	M21	A26
CB2_BUS[26]	IO_VB3N1_N23	N23	A27
CB2_BUS[27]	IO_VB3N1_J24	J24	A28
CB2_BUS[28]	IO_VB3N2_E27	E27	A29
CB2_BUS[29]	IO_VB3N3_G28	G28	A30
CB2_BUS[30]	PLL5_OUT1p	B18	A31
CB2_BUS[31]	PLL5_OUT1n	C18	A32
CB2_BUS[32]	IO_VB3N0_B24	B24	B1
CB2_BUS[33]	IO_VB3N0_A23	A23	B2
CB2_BUS[34]	IO_VB3N1_B25	B25	B3
CB2_BUS[35]	IO_VB3N1_C25	C25	B4
CB2_BUS[36]	IO_VB3N1_A26	A26	B5
CB2_BUS[37]	IO_VB3N1_B26	B26	B6
CB2_BUS[38]	IO_VB3N1_A27	A27	B7
CB2_BUS[39]	IO_VB3N1_B27	B27	B8
CB2_BUS[40]	IO_VB3N2_B28	B28	B9
CB2_BUS[41]	IO_VB3N2_C28	C28	B10
CB2_BUS[42]	IO_VB3N2_D28	D28	B11
CB2_BUS[43]	IO_VB3N2_B29	B29	B12
CB2_BUS[44]	IO_VB3N2_A30	A30	B13
CB2_BUS[45]	IO_VB3N2_B30	B30	B14
CB2_BUS[46]	IO_VB3N3_B31	B31	B15
CB2_BUS[47]	IO_VB3N3_C31	C31	B16
CB2_BUS[48]	IO_VB3N3_D31	D31	B17
CB2_BUS[49]	IO_VB3N3_B32	B32	B18
CB2_BUS[50]	IO_VB3N3_B33	B33	B19
CB2_BUS[51]	IO_VB3N3_A33	A33	B20
CB2_BUS[52]	IO_VB3N4_B34	B34	B21
CB2_BUS[53]	IO_VB3N4_B35	B35	B22
CB2_BUS[54]	IO_VB3N4_C35	C35	B23
CB2_BUS[55]	IO_VB3N4_C34	C34	B24
CB2_BUS[56]	IO_VB3N1_H23	H23	B25
CB2_BUS[57]	IO_VB3N1_M22	M22	B26
CB2_BUS[58]	IO_VB3N2_N24	N24	B27
CB2_BUS[59]	IO_VB3N2_J26	J26	B28
CB2_BUS[60]	IO_VB3N3_M27	M27	B29
CB2_BUS[61]	IO_VB3N3_N27	N27	B30
CB2_BUS[62]	PLL5_FBp	D18	B31
CB2_BUS[62]	PLL5_FBp	D18	B31
CB2_BUS[63]	PLL5_FBn	E18	B32
CB2_BUS[63]	PLL5_FBn	E18	B32
CB2_CLK+	PLL5_OUT0p	A19	A49

CB2_CLK-	PLL5_OUT0n	B19	A50
CB2_IO[0]	IO_VB3N3_E29	E29	A53
CB2_IO[1]	IO_VB3N4_E30	E30	A54
CB2_IO[2]	IO_VB3N2_F26	F26	A55
CB2_IO[3]	IO_VB3N3_F27	F27	A56
CB2_IO[4]	IO_VB3N0_G23	G23	A57
CB2_IO[5]	IO_VB3N1_G24	G24	A58
CB2_IO[6]	IO_VB3N3_G27	G27	A59
CB2_IO[7]	IO_VB3N4_G29	G29	A60
CB2_IO[8]	IO_VB3N2_H26	H26	A61
CB2_IO[9]	IO_VB3N3_H27	H27	A62
CB2_IO[10]	IO_VB3N2_J25	J25	A63
CB2_IO[11]	IO_VB3N3_J27	J27	A64
CB2_IO[12]	IO_VB3N1_K24	K24	A65
CB2_IO[13]	IO_VB3N2_K25	K25	A66
CB2_IO[14]	IO_VB3N4_M28	M28	B34
CB2_IO[15]	IO_VB3N1_E24	E24	B49
CB2_IO[16]	IO_VB3N1_E25	E25	B50
CB2_IO[17]	IO_VB3N1_E26	E26	B51
CB2_IO[18]	IO_VB3N2_E28	E28	B52
CB2_IO[19]	IO_VB3N0_F23	F23	B53
CB2_IO[20]	IO_VB3N1_F24	F24	B54
CB2_IO[21]	IO_VB3N4_F29	F29	B55
CB2_IO[22]	IO_VB3N4_F30	F30	B56
CB2_IO[23]	IO_VB3N2_G25	G25	B57
CB2_IO[24]	IO_VB3N2_G26	G26	B58
CB2_IO[25]	IO_VB3N1_H24	H24	B59
CB2_IO[26]	IO_VB3N2_H25	H25	B60
CB2_IO[27]	IO_VB3N4_H28	H28	B61
CB2_IO[28]	IO_VB3N1_J23	J23	B62
CB2_IO[29]	IO_VB3N4_J28	J28	B63
CB2_IO[30]	IO_VB3N1_K23	K23	B64
CB2_IO[31]	IO_VB3N2_K26	K26	B65
CB2_IO[32]	IO_VB3N3_K27	K27	B66

Table 7.21: Pin connection to the *Hpe_childboard* 2 connector.

Additionally to the signal *CB2_CLK** there are two more differential pairs: *CB2_BUS[30]* and *CB2_BUS[31]* is one differential signal pair where *CB2_BUS[30]* is the positive part and *CB2_BUS[62]* and *CB2_BUS[63]* is the other differential signal pair where *CB2_BUS[62]* is the positive part. The differential signals are connected to PLL output pins of the PLL 6. The signal pair *CB2_BUS[62]*/*CB2_BUS[63]* is additionally connected to the feedback pin of PLL 12.

7.10 Connector to the Mainboard

The following description is based on the presumption that the *Hpe_midi* is used as a mainboard. For a detailed description of the pins, refer to the manual of the *Hpe_midi*.

7.10.1 Audio Interface (AC97)

The signals in table 7.22 are connected to the AC97 on the mainboard.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
AC97_BITCLK	CLK4n	AT20
AC97_EAPD	IO_VB1N2_AF35	AF35
AC97_EXT_CLK	PLL11_FBp	D22
AC97_RESET#	IO_VB1N2_AG34	AG34
AC97_SDATA_IN	IO_VB1N2_AG36	AG36
AC97_SDATA_OUT	IO_VB1N2_AG33	AG33
AC97_SYNC	IO_VB1N2_AF34	AF34

Table 7.22: Pin connection to the module connector: AC97.

The signal *AC97_EXT_CLK* is connected to a PLL output pin of the PLL 11.

7.10.2 A/D Converter (ADC) and D/A Converter (DAC)

The signals in table 7.23 are connected to the ADC/DAC on the mainboard.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
ADC_AIN	IO_VB8N0_AR28	AR28
ADC_DOUT	IO_VB8N0_AN29	AN29
ADC_DOUT#	IO_VB8N0_AP29	AP29
DAC_OUT	IO_VB8N0_AR29	AR29

Table 7.23: Pin connection to the module connector: ADC/DAC.

7.10.3 CAN Interface

The signals in table 7.24 are connected to the CAN on the mainboard.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
CAN_RXD	IO_VB8N0_AU35	AU35
CAN_STB	IO_VB8N0_AV34	AV34
CAN_TXD	IO_VB8N0_AU34	AU34

Table 7.24: Pin connection to the module connector: CAN.

7.10.4 External User Interface

The signals in table 7.25 are connected to the external user interface on the mainboard.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
DSW[0]	IO_VB1N3_AF28	AF28
DSW[1]	IO_VB1N3_AG27	AG27

DSW[2]	IO_VB1N3_AG28	AG28
DSW[3]	IO_VB1N3_AG29	AG29
DSW[4]	IO_VB1N3_AG30	AG30
DSW[5]	IO_VB1N3_AG31	AG31
DSW[6]	IO_VB1N3_AG32	AG32
DSW[7]	IO_VB1N3_AH28	AH28

Table 7.25: Pin connection to the module connector: external user interface.

7.10.5 Ethernet Interface

The signals in table 7.26 are connected to the Ethernet on the mainboard.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
ETH_COL	IO_VB1N2_AK37	AK37
ETH_CRS	IO_VB1N2_AK36	AK36
ETH_MDC	IO_VB1N3_AE26	AE26
ETH_MDINTR#	IO_VB1N2_AM39	AM39
ETH_MDIO	IO_VB1N3_AE27	AE27
ETH_RESET#	IO_VB1N3_AF27	AF27
ETH_RXCLK	CLK5p	AU21
ETH_RXDV	IO_VB1N2_AJ37	AJ37
ETH_RXD[0]	IO_VB1N2_AM38	AM38
ETH_RXD[1]	IO_VB1N2_AL39	AL39
ETH_RXD[2]	IO_VB1N2_AL38	AL38
ETH_RXD[3]	IO_VB1N2_AL37	AL37
ETH_RXER	IO_VB1N2_AL36	AL36
ETH_TXCLK	CLK4p	AU20
ETH_TXD[0]	IO_VB1N2_AH37	AH37
ETH_TXD[1]	IO_VB1N2_AH36	AH36
ETH_TXD[2]	IO_VB1N2_AH35	AH35
ETH_TXD[3]	IO_VB1N2_AH34	AH34
ETH_TXEN	IO_VB1N2_AJ36	AJ36
ETH_TXER	IO_VB1N2_AG37	AG37

Table 7.26: Pin connection to the module connector: Ethernet.

The signal *ETH_TXCLK* is connected to the clock input pin 4 and the signal *ETH_RXCLK* is connected to the clock input pin 5.

7.10.6 Expansion Connector

The signals in table 7.27 are connected to the expansion connector on the mainboard.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
EXPCON_CLKIN	PLL11_FBn	E22
EXPCON_CLKOUT	CLK2n	Y38
CARDSEL#	IO_VB8N0_AJ28	AJ28

Table 7.27: Pin connection to the module connector: expansion connector.

7.10.7 Parallel Flash

The signals in table 7.28 are connected to the flash on the mainboard.

Signal Name	FPGA Pin Name	FPGA Pin Number
FLASH_BYTE#	IO_VB8N3_AU26	AU26
FLASH_CE#	IO_VB8N3_AP24	AP24
FLASH_RESET#	IO_VB8N3_AT25	AT25
FLASH_RY/BY#_A	IO_VB8N3_AT26	AT26
FLASH_RY/BY#_B	IO_VB8N3_AT27	AT27
FLASH_WP#/ACC	IO_VB8N3_AU25	AU25

Table 7.28: Pin connection to the module connector: flash.

7.10.8 Human Interface

The signals in table 7.29 are connected to the 7-segment display, DIP switches and LEDs on the mainboard.

Signal Name	FPGA Pin Name	FPGA Pin Number
HUMI_A#	IO_VB1N3_AM37	AM37
HUMI_B#	IO_VB1N3_AN36	AN36
HUMI_C#	IO_VB1N3_AN37	AN37
HUMI_DP#	IO_VB1N3_AR38	AR38
HUMI_D#	IO_VB1N3_AN38	AN38
HUMI_E#	IO_VB1N3_AN39	AN39
HUMI_F#	IO_VB1N3_AP38	AP38
HUMI_G#	IO_VB1N3_AP39	AP39
HUMI_LED#	IO_VB1N3_AL34	AL34
HUMI_SEG0#	IO_VB1N3_AL35	AL35
HUMI_SEG1#	IO_VB1N3_AM36	AM36

Table 7.29: Pin connection to the module connector: human interface.

7.10.9 I^2C

The signals in table 7.30 are connected to the I^2C on the mainboard.

Signal Name	FPGA Pin Name	FPGA Pin Number
I2C_SCL[1]	IO_VB8N0_AL28	AL28
I2C_SDA[1]	IO_VB8N0_AK28	AK28

Table 7.30: Pin connection to the module connector: I^2C.

7.10.10 LCD Connector

The signals in table 7.31 are connected to the LCD on the mainboard.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
LCD_ENABLE	IO_VB8N0_AN28	AN28
LCD_REGSEL	IO_VB8N0_AM28	AM28
LCD_RW	IO_VB8N0_AM29	AM29

Table 7.31: Pin connection to the module connector: LCD.

7.10.11 LIN Interface

The signals in table 7.32 are connected to the LIN on the mainboard.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
LIN_ACTIVE#	IO_VB8N0_AV35	AV35
LIN_RXD	IO_VB8N0_AW35	AW35
LIN_SLP#	IO_VB8N1_AG26	AG26
LIN_TXD	IO_VB8N0_AW34	AW34

Table 7.32: Pin connection to the module connector: LIN.

7.10.12 Memory

The signals in table 7.33 are connected to the memories on the mainboard.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
MEMORY_A[0]	IO_VB8N2_AN26	AN26
MEMORY_A[1]	IO_VB8N2_AR24	AR24
MEMORY_A[2]	IO_VB8N2_AR25	AR25
MEMORY_A[3]	IO_VB8N2_AT28	AT28
MEMORY_A[4]	IO_VB8N2_AT29	AT29
MEMORY_A[5]	IO_VB8N2_AT30	AT30
MEMORY_A[6]	IO_VB8N2_AU28	AU28
MEMORY_A[7]	IO_VB8N2_AU29	AU29
MEMORY_A[8]	IO_VB8N2_AU30	AU30
MEMORY_A[9]	IO_VB8N2_AV28	AV28
MEMORY_A[10]	IO_VB8N2_AV29	AV29
MEMORY_A[11]	IO_VB8N2_AV30	AV30
MEMORY_A[12]	IO_VB8N2_AW28	AW28
MEMORY_A[13]	IO_VB8N2_AW29	AW29
MEMORY_A[14]	IO_VB8N2_AW30	AW30
MEMORY_A[15]	IO_VB8N3_AG22	AG22
MEMORY_A[16]	IO_VB8N3_AG23	AG23
MEMORY_A[17]	IO_VB8N3_AH22	AH22

MEMORY_A[18]	IO_VB8N3_AH23	AH23
MEMORY_A[19]	IO_VB8N3_AJ23	AJ23
MEMORY_A[20]	IO_VB8N3_AJ24	AJ24
MEMORY_A[21]	IO_VB8N3_AL23	AL23
MEMORY_A[22]	IO_VB8N3_AL24	AL24
MEMORY_DQ[0]	IO_VB8N1_AJ27	AJ27
MEMORY_DQ[1]	IO_VB8N1_AK27	AK27
MEMORY_DQ[2]	IO_VB8N1_AL27	AL27
MEMORY_DQ[3]	IO_VB8N1_AM27	AM27
MEMORY_DQ[4]	IO_VB8N1_AN27	AN27
MEMORY_DQ[5]	IO_VB8N1_AP26	AP26
MEMORY_DQ[6]	IO_VB8N1_AP27	AP27
MEMORY_DQ[7]	IO_VB8N1_AR26	AR26
MEMORY_DQ[8]	IO_VB8N1_AR27	AR27
MEMORY_DQ[9]	IO_VB8N1_AT31	AT31
MEMORY_DQ[10]	IO_VB8N1_AT32	AT32
MEMORY_DQ[11]	IO_VB8N1_AT33	AT33
MEMORY_DQ[12]	IO_VB8N1_AU31	AU31
MEMORY_DQ[13]	IO_VB8N1_AU32	AU32
MEMORY_DQ[14]	IO_VB8N1_AU33	AU33
MEMORY_DQ[15]	IO_VB8N1_AV31	AV31
MEMORY_DQ[16]	IO_VB8N1_AV32	AV32
MEMORY_DQ[17]	IO_VB8N1_AV33	AV33
MEMORY_DQ[18]	IO_VB8N1_AW31	AW31
MEMORY_DQ[19]	IO_VB8N1_AW32	AW32
MEMORY_DQ[20]	IO_VB8N1_AW33	AW33
MEMORY_DQ[21]	IO_VB8N2_AG24	AG24
MEMORY_DQ[22]	IO_VB8N2_AG25	AG25
MEMORY_DQ[23]	IO_VB8N2_AH24	AH24
MEMORY_DQ[24]	IO_VB8N2_AH25	AH25
MEMORY_DQ[25]	IO_VB8N2_AJ25	AJ25
MEMORY_DQ[26]	IO_VB8N2_AJ26	AJ26
MEMORY_DQ[27]	IO_VB8N2_AK25	AK25
MEMORY_DQ[28]	IO_VB8N2_AK26	AK26
MEMORY_DQ[29]	IO_VB8N2_AL25	AL25
MEMORY_DQ[30]	IO_VB8N2_AL26	AL26
MEMORY_DQ[31]	IO_VB8N2_AM25	AM25
MEMORY_OE#	IO_VB8N2_AM26	AM26
MEMORY_WE#	IO_VB8N2_AN25	AN25

Table 7.33: Pin connection to the module connector: memories.

7.10.13 PS/2 Ports

The signals in table 7.34 are connected to the PS/2 on the mainboard.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
PS2_KBCLK	PLL11_OUT0p	A21
PS2_KBDAT	PLL11_OUT0n	B21

PS2_MCLK	PLL11_OUT1p	B22
PS2_MDAT	PLL11_OUT1n	C22

Table 7.34: Pin connection to the module connector: PS/2.

The signals *PS2_KBCLK* and *PS2_MCLK* are connected to PLL output pins of the PLL 11.

7.10.14 Serial Interface (RS232)

The signals in table 7.35 are connected to the RS232 on the mainboard.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
RS0_CTS_LVTTL	IO_VB8N4_AL22	AL22
RS0_RTS_LVTTL	IO_VB8N3_AK23	AK23
RS0_RXD_LVTTL	IO_VB8N3_AK24	AK24
RS0_TXD_LVTTL	IO_VB8N4_AJ22	AJ22
RS1_CTS_LVTTL	IO_VB8N4_AP20	AP20
RS1_RTS_LVTTL	IO_VB8N4_AM22	AM22
RS1_RXD_LVTTL	IO_VB8N4_AN22	AN22
RS1_TXD_LVTTL	IO_VB8N4_AM21	AM21

Table 7.35: Pin connection to the module connector: RS232.

7.10.15 SD Card Reader

The signals in table 7.36 are connected to the SD card on the mainboard.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
SDCARD_CD	IO_VB8N3_AW27	AW27
SDCARD_CS	IO_VB8N3_AU27	AU27
SDCARD_CT	IO_VB8N4_AG21	AG21
SDCARD_DAT	IO_VB8N3_AW26	AW26
SDCARD_DI	IO_VB8N3_AV25	AV25
SDCARD_DO	IO_VB8N3_AV27	AV27
SDCARD_IRQ	IO_VB8N3_AW25	AW25
SDCARD_SCLK	IO_VB8N3_AV26	AV26
SDCARD_WRP	IO_VB8N4_AH21	AH21

Table 7.36: Pin connection to the module connector: SD card.

7.10.16 Asynchronous SRAM

The signals in table 7.37 are connected to the SRAM on the mainboard.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
SRAM_BE0#	IO_VB8N3_AM23	AM23

SRAM_BE1#	IO_VB8N3_AM24	AM24
SRAM_BE2#	IO_VB8N3_AN23	AN23
SRAM_BE3#	IO_VB8N3_AN24	AN24
SRAM_CE#	IO_VB8N3_AP23	AP23

Table 7.37: Pin connection to the module connector: SRAM.

7.10.17 3 x 4 Key Matrix

The signals in table 7.38 are connected to the key matrix on the mainboard.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
TST_COL[0]	IO_VB1N3_AJ32	AJ32
TST_COL[1]	IO_VB1N3_AJ33	AJ33
TST_COL[2]	IO_VB1N3_AJ34	AJ34
TST_COL[3]	IO_VB1N3_AJ35	AJ35
TST_COL[4]	IO_VB1N3_AK34	AK34
TST_COL[5]	IO_VB1N3_AK35	AK35
TST_ROW[0]	IO_VB1N3_AH30	AH30
TST_ROW[1]	IO_VB1N3_AH31	AH31
TST_ROW[2]	IO_VB1N3_AH32	AH32
TST_ROW[3]	IO_VB1N3_AH33	AH33
TST_STEP	IO_VB1N3_AH29	AH29

Table 7.38: Pin connection to the module connector: key matrix.

7.10.18 USB Target Connector

The signals in table 7.39 are connected to the USB target for debugging on the mainboard.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
USBD_CLKOUT	CLK2p	Y39
USBD_DBUS16_8	IO_VB1N1_AJ38	AJ38
USBD_D[0]	IO_VB1N1_AK38	AK38
USBD_D[10]	IO_VB1N2_AE32	AE32
USBD_D[11]	IO_VB1N2_AE33	AE33
USBD_D[12]	IO_VB1N2_AE34	AE34
USBD_D[13]	IO_VB1N2_AE35	AE35
USBD_D[14]	IO_VB1N2_AF29	AF29
USBD_D[15]	IO_VB1N2_AF30	AF30
USBD_D[1]	IO_VB1N1_AK39	AK39
USBD_D[2]	IO_VB1N2_AD26	AD26
USBD_D[3]	IO_VB1N2_AD27	AD27
USBD_D[4]	IO_VB1N2_AD28	AD28
USBD_D[5]	IO_VB1N2_AD29	AD29
USBD_D[6]	IO_VB1N2_AE28	AE28
USBD_D[7]	IO_VB1N2_AE29	AE29

USBD_D[8]	IO_VB1N2_AE30	AE30
USBD_D[9]	IO_VB1N2_AE31	AE31
USBD_LINESTATE[0]	IO_VB1N1_AH38	AH38
USBD_LINESTATE[1]	IO_VB1N1_AH39	AH39
USBD_OPMODE[0]	IO_VB1N1_AF37	AF37
USBD_OPMODE[1]	IO_VB1N1_AF38	AF38
USBD_RESET	IO_VB1N2_AF33	AF33
USBD_RXACTIVE	IO_VB1N1_AE37	AE37
USBD_RXERROR	IO_VB1N1_AF36	AF36
USBD_RXVALID	IO_VB1N1_AE36	AE36
USBD_SUSPEND	IO_VB1N1_AG39	AG39
USBD_TERMSEL	IO_VB1N1_AG38	AG38
USBD_TXREADY	IO_VB1N1_AD35	AD35
USBD_TXVALID	IO_VB1N1_AD34	AD34
USBD_UNIBIDI	IO_VB1N1_AJ39	AJ39
USBD_VALIDH	IO_VB1N1_AD36	AD36
USBD_VBUS	IO_VB1N2_AF32	AF32
USBD_XCRSEL	IO_VB1N1_AF39	AF39

Table 7.39: Pin connection to the module connector: USB target.

The signal *USBD_CLKOUT* is connected to the clock input pin 2.

7.10.19 USB Host and On The Go (OTG) Connector

The signals in table 7.40 are connected to the USB OTB on the mainboard.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
USB_CTS	IO_VB1N1_AC29	AC29
USB_GPIO[0]	IO_VB1N0_Y32	Y32
USB_GPIO[10]	IO_VB1N0_AA32	AA32
USB_GPIO[11]	IO_VB1N0_AA33	AA33
USB_GPIO[12]	IO_VB1N0_AA36	AA36
USB_GPIO[13]	IO_VB1N0_AA37	AA37
USB_GPIO[14]	IO_VB1N0_AA38	AA38
USB_GPIO[15]	IO_VB1N0_AA39	AA39
USB_GPIO[16]	IO_VB1N0_AB29	AB29
USB_GPIO[17]	IO_VB1N0_AB30	AB30
USB_GPIO[18]	IO_VB1N0_AB35	AB35
USB_GPIO[19]	IO_VB1N0_AB36	AB36
USB_GPIO[1]	IO_VB1N0_Y33	Y33
USB_GPIO[20]	IO_VB1N0_AB37	AB37
USB_GPIO[21]	IO_VB1N0_AB38	AB38
USB_GPIO[22]	IO_VB1N0_AC38	AC38
USB_GPIO[23]	IO_VB1N0_AC39	AC39
USB_GPIO[24]	IO_VB1N0_AD37	AD37
USB_GPIO[25]	IO_VB1N0_AD38	AD38
USB_GPIO[26]	IO_VB1N0_AE38	AE38
USB_GPIO[27]	IO_VB1N0_AE39	AE39
USB_GPIO[28]	IO_VB1N1_AB27	AB27

USB_GPIO[2]	IO_VB1N0_Y34	Y34
USB_GPIO[3]	IO_VB1N0_Y35	Y35
USB_GPIO[4]	IO_VB1N0_AA26	AA26
USB_GPIO[5]	IO_VB1N0_AA27	AA27
USB_GPIO[6]	IO_VB1N0_AA28	AA28
USB_GPIO[7]	IO_VB1N0_AA29	AA29
USB_GPIO[8]	IO_VB1N0_AA30	AA30
USB_GPIO[9]	IO_VB1N0_AA31	AA31
USB_MISO	IO_VB1N1_AB28	AB28
USB_MOSI	IO_VB1N1_AB33	AB33
USB_OC0#	IO_VB1N1_AC33	AC33
USB_OC1#	IO_VB1N1_AC36	AC36
USB_OC2#	IO_VB1N1_AD31	AD31
USB_OC3#	IO_VB1N1_AD33	AD33
USB_PWEN[0]	IO_VB1N1_AC32	AC32
USB_PWEN[1]	IO_VB1N1_AC34	AC34
USB_PWEN[2]	IO_VB1N1_AC37	AC37
USB_PWEN[3]	IO_VB1N1_AD32	AD32
USB_RTS	IO_VB1N1_AC28	AC28
USB_RXD	IO_VB1N1_AC27	AC27
USB_SCK	IO_VB1N1_AB32	AB32
USB_SCL	IO_VB1N1_AC30	AC30
USB_SDA	IO_VB1N1_AC31	AC31
USB_SSI#	IO_VB1N1_AB31	AB31
USB_TXD	IO_VB1N1_AB34	AB34

Table 7.40: Pin connection to the module connector: USB OTG.

7.10.20 VGA Interface

The signals in table 7.41 are connected to the VGA on the mainboard.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
VGA_BLANK#	IO_VB1N4_AU37	AU37
VGA_BL[0]	IO_VB1N4_AJ31	AJ31
VGA_BL[1]	IO_VB1N4_AK31	AK31
VGA_BL[2]	IO_VB1N4_AT36	AT36
VGA_BL[3]	IO_VB1N4_AT37	AT37
VGA_BL[4]	IO_VB1N4_AU36	AU36
VGA_BL[5]	IO_VB1N4_AM34	AM34
VGA_BL[6]	IO_VB1N4_AM35	AM35
VGA_BL[7]	IO_VB1N4_AN33	AN33
VGA_CLK	IO_VB1N4_AP35	AP35
VGA_GR[0]	IO_VB1N3_AV38	AV38
VGA_GR[1]	IO_VB1N4_AJ30	AJ30
VGA_GR[2]	IO_VB1N4_AR37	AR37
VGA_GR[3]	IO_VB1N4_AT34	AT34
VGA_GR[4]	IO_VB1N4_AT35	AT35
VGA_GR[5]	IO_VB1N4_AL32	AL32

VGA_GR[6]	IO_VB1N4_AM31	AM31
VGA_GR[7]	IO_VB1N4_AM32	AM32
VGA_HSYNC	IO_VB1N4_AN34	AN34
VGA_RD[0]	IO_VB1N3_AR39	AR39
VGA_RD[1]	IO_VB1N3_AV37	AV37
VGA_RD[2]	IO_VB1N4_AP37	AP37
VGA_RD[3]	IO_VB1N4_AR34	AR34
VGA_RD[4]	IO_VB1N4_AR35	AR35
VGA_RD[5]	IO_VB1N4_AR36	AR36
VGA_RD[6]	IO_VB1N4_AK32	AK32
VGA_RD[7]	IO_VB1N4_AL31	AL31
VGA_SYNC#	IO_VB1N4_AP36	AP36
VGA_VSYNC	IO_VB1N4_AP34	AP34

Table 7.41: Pin connection to the module connector: VGA.

7.10.21 System Reset

The signals in table 7.42 are also connected to the mainboard.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
USER_RESET#	IO_VB8N1_AH27	AH27
HPE_RESOUT#	IO_VB8N1_AH26	AH26

Table 7.42: Pin connection to the module connector: Other pins.

The signal *HPE_RESOUT#* is an output of the FPGA and resets devices on the mainboard. The signal *USER_RESET#* is connected to the push button on the front panel. This signal is only connected to the *DUT-FPGA#1*. If you want to use *USER_RESET#* on the *DUT-FPGA#2* as well, you have to deliver it via the connection between the FPGAs (refer to section 7.2 and 8.2).

Attention: When you use the *USER_RESET#*, you have to add a pull up resistor into the PAD of the FPGA!

7.10.22 Power Reset

The signal *PWR_RESET#* table 7.43 is the global reset signal for the whole system. It is delivered via the module connector. The reset is low active, activated after power up and controlled by a supervisor on the *Hpe_midi*.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
PWR_RESET#	DEV_CLRn	AN21

Table 7.43: Pin connection to the module connector: Global Reset.

8 FPGA DUT#2

You find a file with the lengths of all signals on your data disc.

Generally, all signals named *- and *+ are differential signals where only the signal named *+ is addressed when using the LVDS standard. However, if the signal is used in a single ended standard, both *- and *+ can be used independently.

A signal with a # in its name is low active.

8.1 PLLs

PLL 5 is driven with 2.5 V by default. However, if it is necessary (e.g. for LVDS clocks) there is the possibility to change the power supply to 3.3 V via a resistor jumper (stuff RJ34 instead of RJ33 with a 0 ohm resistor).

PLL 6, PLL 11 and PLL 12 are always supplied with 3.3 V.

8.2 Connection to DUT-FPGA#1

A bus of 512 bits width is established between the two DUT-FGPAs. It is possible to measure high-impedance ('Z') on 128 lines of this bus. Additionally, a LVDS connection of 32 differential pairs per direction is available.

In table 8.1 the 512-bit bus connection to *DUT-FPGA#1* can be found. The signals, on which a 'Z' measuring is possible are *emphasised*.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
DATA_BUS[0]	IO_VB1N2_AD26	AD26
DATA_BUS[1]	IO_VB1N2_AD27	AD27
DATA_BUS[2]	IO_VB1N2_AE28	AE28
DATA_BUS[3]	IO_VB1N2_AE29	AE29
DATA_BUS[4]	IO_VB1N2_AE30	AE30
DATA_BUS[5]	IO_VB1N2_AE31	AE31
DATA_BUS[6]	IO_VB1N2_AE32	AE32
DATA_BUS[7]	IO_VB1N2_AE33	AE33
DATA_BUS[8]	IO_VB1N2_AE34	AE34
DATA_BUS[9]	IO_VB1N2_AE35	AE35
DATA_BUS[10]	IO_VB1N2_AF29	AF29
DATA_BUS[11]	IO_VB1N2_AF30	AF30
DATA_BUS[12]	IO_VB1N2_AF32	AF32
DATA_BUS[13]	IO_VB1N2_AF33	AF33
DATA_BUS[14]	IO_VB1N2_AF34	AF34
DATA_BUS[15]	IO_VB1N2_AF35	AF35
DATA_BUS[16]	IO_VB1N2_AG33	AG33
DATA_BUS[17]	IO_VB1N2_AG34	AG34
DATA_BUS[18]	IO_VB1N2_AH34	AH34
DATA_BUS[19]	IO_VB1N2_AH35	AH35
DATA_BUS[20]	IO_VB1N2_AH36	AH36
DATA_BUS[21]	IO_VB1N2_AH37	AH37

DATA_BUS[22]	IO_VB1N2_AJ36	AJ36
DATA_BUS[23]	IO_VB1N2_AJ37	AJ37
DATA_BUS[24]	IO_VB1N2_AK36	AK36
DATA_BUS[25]	IO_VB1N2_AK37	AK37
DATA_BUS[26]	IO_VB1N2_AL36	AL36
DATA_BUS[27]	IO_VB1N2_AL37	AL37
DATA_BUS[28]	IO_VB1N2_AL38	AL38
DATA_BUS[29]	IO_VB1N2_AL39	AL39
DATA_BUS[30]	IO_VB1N2_AM38	AM38
DATA_BUS[31]	IO_VB1N2_AM39	AM39
DATA_BUS[32]	IO_VB1N3_AE26	AE26
DATA_BUS[33]	IO_VB1N3_AE27	AE27
DATA_BUS[34]	IO_VB1N3_AF27	AF27
DATA_BUS[35]	IO_VB1N3_AF28	AF28
DATA_BUS[36]	IO_VB1N3_AG27	AG27
DATA_BUS[37]	IO_VB1N3_AG28	AG28
DATA_BUS[38]	IO_VB1N3_AG29	AG29
DATA_BUS[39]	IO_VB1N3_AG30	AG30
DATA_BUS[40]	IO_VB1N3_AG31	AG31
DATA_BUS[41]	IO_VB1N3_AG32	AG32
DATA_BUS[42]	IO_VB1N3_AH28	AH28
DATA_BUS[43]	IO_VB1N3_AH29	AH29
DATA_BUS[44]	IO_VB1N3_AH30	AH30
DATA_BUS[45]	IO_VB1N3_AH31	AH31
DATA_BUS[46]	IO_VB1N3_AH32	AH32
DATA_BUS[47]	IO_VB1N3_AH33	AH33
DATA_BUS[48]	IO_VB1N3_AJ32	AJ32
DATA_BUS[49]	IO_VB1N3_AJ33	AJ33
DATA_BUS[50]	IO_VB1N3_AJ34	AJ34
DATA_BUS[51]	IO_VB1N3_AJ35	AJ35
DATA_BUS[52]	IO_VB1N3_AK34	AK34
DATA_BUS[53]	IO_VB1N3_AK35	AK35
DATA_BUS[54]	IO_VB1N3_AL34	AL34
DATA_BUS[55]	IO_VB1N3_AL35	AL35
DATA_BUS[56]	IO_VB1N3_AM36	AM36
DATA_BUS[57]	IO_VB1N3_AM37	AM37
DATA_BUS[58]	IO_VB1N3_AN36	AN36
DATA_BUS[59]	IO_VB1N3_AN37	AN37
DATA_BUS[60]	IO_VB1N3_AN38	AN38
DATA_BUS[61]	IO_VB1N3_AN39	AN39
DATA_BUS[62]	IO_VB1N3_AP38	AP38
DATA_BUS[63]	IO_VB1N3_AP39	AP39
DATA_BUS[64]	IO_VB1N3_AR38	AR38
DATA_BUS[65]	IO_VB1N3_AR39	AR39
DATA_BUS[66]	IO_VB1N3_AV37	AV37
DATA_BUS[67]	IO_VB1N3_AV38	AV38
DATA_BUS[68]	IO_VB1N4_AJ30	AJ30
DATA_BUS[69]	IO_VB1N4_AJ31	AJ31
DATA_BUS[70]	IO_VB1N4_AK31	AK31
DATA_BUS[71]	IO_VB1N4_AK32	AK32
DATA_BUS[72]	IO_VB1N4_AL31	AL31

DATA_BUS[73]	IO_VB1N4_AL32	AL32
DATA_BUS[74]	IO_VB1N4_AM31	AM31
DATA_BUS[75]	IO_VB1N4_AM32	AM32
DATA_BUS[76]	IO_VB1N4_AM34	AM34
DATA_BUS[77]	IO_VB1N4_AM35	AM35
DATA_BUS[78]	IO_VB1N4_AN33	AN33
DATA_BUS[79]	IO_VB1N4_AN34	AN34
DATA_BUS[80]	IO_VB1N4_AP34	AP34
DATA_BUS[81]	IO_VB1N4_AP35	AP35
DATA_BUS[82]	IO_VB1N4_AP36	AP36
DATA_BUS[83]	IO_VB1N4_AP37	AP37
DATA_BUS[84]	IO_VB1N4_AR34	AR34
DATA_BUS[85]	IO_VB1N4_AR35	AR35
DATA_BUS[86]	IO_VB1N4_AR36	AR36
DATA_BUS[87]	IO_VB1N4_AR37	AR37
DATA_BUS[88]	IO_VB1N4_AT34	AT34
DATA_BUS[89]	IO_VB1N4_AT35	AT35
DATA_BUS[90]	IO_VB1N4_AT36	AT36
DATA_BUS[91]	IO_VB1N4_AT37	AT37
DATA_BUS[92]	IO_VB1N4_AU36	AU36
DATA_BUS[93]	IO_VB1N4_AU37	AU37
DATA_BUS[94]	IO_VB2N0_C36	C36
DATA_BUS[95]	IO_VB2N0_C37	C37
DATA_BUS[96]	IO_VB2N0_J31	J31
DATA_BUS[97]	IO_VB2N0_J32	J32
DATA_BUS[98]	IO_VB2N0_L30	L30
DATA_BUS[99]	IO_VB2N0_L31	L31
DATA_BUS[100]	IO_VB2N1_B37	B37
DATA_BUS[101]	IO_VB2N1_B38	B38
DATA_BUS[102]	IO_VB2N1_D36	D36
DATA_BUS[103]	IO_VB2N1_D37	D37
DATA_BUS[104]	IO_VB2N1_E34	E34
DATA_BUS[105]	IO_VB2N1_E35	E35
DATA_BUS[106]	IO_VB2N1_E36	E36
DATA_BUS[107]	IO_VB2N1_E37	E37
DATA_BUS[108]	IO_VB2N1_E38	E38
DATA_BUS[109]	IO_VB2N1_E39	E39
DATA_BUS[110]	IO_VB2N1_F34	F34
DATA_BUS[111]	IO_VB2N1_F35	F35
DATA_BUS[112]	IO_VB2N1_F36	F36
DATA_BUS[113]	IO_VB2N1_F37	F37
DATA_BUS[114]	IO_VB2N1_G34	G34
DATA_BUS[115]	IO_VB2N1_G35	G35
DATA_BUS[116]	IO_VB2N1_H31	H31
DATA_BUS[117]	IO_VB2N1_H32	H32
DATA_BUS[118]	IO_VB2N1_H34	H34
DATA_BUS[119]	IO_VB2N1_H35	H35
DATA_BUS[120]	IO_VB2N1_J33	J33
DATA_BUS[121]	IO_VB2N1_J34	J34
DATA_BUS[122]	IO_VB2N1_K31	K31
DATA_BUS[123]	IO_VB2N1_K32	K32

DATA_BUS[124]	IO_VB2N1_K34	K34
DATA_BUS[125]	IO_VB2N1_K35	K35
DATA_BUS[126]	IO_VB2N1_L32	L32
DATA_BUS[127]	IO_VB2N1_L33	L33
DATA_BUS[128]	IO_VB2N1_M30	M30
DATA_BUS[129]	IO_VB2N1_M31	M31
DATA_BUS[130]	IO_VB2N1_M32	M32
DATA_BUS[131]	IO_VB2N1_M33	M33
DATA_BUS[132]	IO_VB2N1_N28	N28
DATA_BUS[133]	IO_VB2N1_N29	N29
DATA_BUS[134]	IO_VB2N1_N30	N30
DATA_BUS[135]	IO_VB2N1_N31	N31
DATA_BUS[136]	IO_VB2N2_J36	J36
DATA_BUS[137]	IO_VB2N2_J37	J37
DATA_BUS[138]	IO_VB2N2_K36	K36
DATA_BUS[139]	IO_VB2N2_K37	K37
DATA_BUS[140]	IO_VB2N2_L34	L34
DATA_BUS[141]	IO_VB2N2_L35	L35
DATA_BUS[142]	IO_VB2N2_L36	L36
DATA_BUS[143]	IO_VB2N2_L37	L37
DATA_BUS[144]	IO_VB2N2_M34	M34
DATA_BUS[145]	IO_VB2N2_M35	M35
DATA_BUS[146]	IO_VB2N2_M36	M36
DATA_BUS[147]	IO_VB2N2_M37	M37
DATA_BUS[148]	IO_VB2N2_N32	N32
DATA_BUS[149]	IO_VB2N2_N33	N33
DATA_BUS[150]	IO_VB2N2_N34	N34
DATA_BUS[151]	IO_VB2N2_N35	N35
DATA_BUS[152]	IO_VB2N2_P26	P26
DATA_BUS[153]	IO_VB2N2_P27	P27
DATA_BUS[154]	IO_VB2N2_P28	P28
DATA_BUS[155]	IO_VB2N2_P29	P29
DATA_BUS[156]	IO_VB2N2_P30	P30
DATA_BUS[157]	IO_VB2N2_P31	P31
DATA_BUS[158]	IO_VB2N2_P32	P32
DATA_BUS[159]	IO_VB2N2_P33	P33
DATA_BUS[160]	IO_VB2N2_R27	R27
DATA_BUS[161]	IO_VB2N2_R28	R28
DATA_BUS[162]	IO_VB2N2_R31	R31
DATA_BUS[163]	IO_VB2N2_R32	R32
DATA_BUS[164]	IO_VB2N2_F38	F38
DATA_BUS[165]	IO_VB2N2_F39	F39
DATA_BUS[166]	IO_VB2N2_G36	G36
DATA_BUS[167]	IO_VB2N2_G37	G37
DATA_BUS[168]	IO_VB2N2_G38	G38
DATA_BUS[169]	IO_VB2N2_G39	G39
DATA_BUS[170]	IO_VB2N2_H36	H36
DATA_BUS[171]	IO_VB2N2_H37	H37
DATA_BUS[172]	IO_VB3N0_A23	A23
DATA_BUS[173]	IO_VB3N0_B23	B23
DATA_BUS[174]	IO_VB3N0_B24	B24

DATA_BUS[175]	IO_VB3N0_C23	C23
DATA_BUS[176]	IO_VB3N0_C24	C24
DATA_BUS[177]	IO_VB3N0_D24	D24
DATA_BUS[178]	IO_VB3N0_F23	F23
DATA_BUS[179]	IO_VB3N0_G23	G23
DATA_BUS[180]	IO_VB3N0_H21	H21
DATA_BUS[181]	IO_VB3N0_J22	J22
DATA_BUS[182]	IO_VB3N0_L22	L22
DATA_BUS[183]	IO_VB3N0_M20	M20
DATA_BUS[184]	IO_VB3N0_M21	M21
DATA_BUS[185]	IO_VB3N0_N21	N21
DATA_BUS[186]	IO_VB3N1_A25	A25
DATA_BUS[187]	IO_VB3N1_A26	A26
DATA_BUS[188]	IO_VB3N1_A27	A27
DATA_BUS[189]	IO_VB3N1_B25	B25
DATA_BUS[190]	IO_VB3N1_B26	B26
DATA_BUS[191]	IO_VB3N1_B27	B27
DATA_BUS[192]	IO_VB3N1_C25	C25
DATA_BUS[193]	IO_VB3N1_C26	C26
DATA_BUS[194]	IO_VB3N1_C27	C27
DATA_BUS[195]	IO_VB3N1_D25	D25
DATA_BUS[196]	IO_VB3N1_D26	D26
DATA_BUS[197]	IO_VB3N1_D27	D27
DATA_BUS[198]	IO_VB3N1_E24	E24
DATA_BUS[199]	IO_VB3N1_E25	E25
DATA_BUS[200]	IO_VB3N1_E26	E26
DATA_BUS[201]	IO_VB3N1_F24	F24
DATA_BUS[202]	IO_VB3N1_G24	G24
DATA_BUS[203]	IO_VB3N1_H23	H23
DATA_BUS[204]	IO_VB3N1_H24	H24
DATA_BUS[205]	IO_VB3N1_J23	J23
DATA_BUS[206]	IO_VB3N1_J24	J24
DATA_BUS[207]	IO_VB3N1_K23	K23
DATA_BUS[208]	IO_VB3N1_K24	K24
DATA_BUS[209]	IO_VB3N1_L23	L23
DATA_BUS[210]	IO_VB3N1_L24	L24
DATA_BUS[211]	IO_VB3N1_M22	M22
DATA_BUS[212]	IO_VB3N1_M23	M23
DATA_BUS[213]	IO_VB3N1_N22	N22
DATA_BUS[214]	IO_VB3N1_N23	N23
DATA_BUS[215]	IO_VB3N2_A28	A28
DATA_BUS[216]	IO_VB3N2_A29	A29
DATA_BUS[217]	IO_VB3N2_A30	A30
DATA_BUS[218]	IO_VB3N2_B28	B28
DATA_BUS[219]	IO_VB3N2_B29	B29
DATA_BUS[220]	IO_VB3N2_B30	B30
DATA_BUS[221]	IO_VB3N2_C28	C28
DATA_BUS[222]	IO_VB3N2_C29	C29
DATA_BUS[223]	IO_VB3N2_C30	C30
DATA_BUS[224]	IO_VB3N2_D28	D28
DATA_BUS[225]	IO_VB3N2_D29	D29

DATA_BUS[226]	IO_VB3N2_D30	D30
DATA_BUS[227]	IO_VB3N2_E27	E27
DATA_BUS[228]	IO_VB3N2_E28	E28
DATA_BUS[229]	IO_VB3N0_F22	F22
DATA_BUS[230]	IO_VB3N2_F26	F26
DATA_BUS[231]	IO_VB3N2_G25	G25
DATA_BUS[232]	IO_VB3N2_G26	G26
DATA_BUS[233]	IO_VB3N2_H25	H25
DATA_BUS[234]	IO_VB3N2_H26	H26
DATA_BUS[235]	IO_VB3N2_J25	J25
DATA_BUS[236]	IO_VB3N2_J26	J26
DATA_BUS[237]	IO_VB3N2_K25	K25
DATA_BUS[238]	IO_VB3N2_K26	K26
DATA_BUS[239]	IO_VB3N2_L25	L25
DATA_BUS[240]	IO_VB3N2_L26	L26
DATA_BUS[241]	IO_VB3N2_M24	M24
DATA_BUS[242]	IO_VB3N2_M25	M25
DATA_BUS[243]	IO_VB3N2_N24	N24
DATA_BUS[244]	IO_VB3N2_N25	N25
DATA_BUS[245]	IO_VB3N3_A31	A31
DATA_BUS[246]	IO_VB3N3_A32	A32
DATA_BUS[247]	IO_VB3N3_A33	A33
DATA_BUS[248]	IO_VB3N3_B31	B31
DATA_BUS[249]	IO_VB3N3_B32	B32
DATA_BUS[250]	IO_VB3N3_B33	B33
DATA_BUS[251]	IO_VB3N3_C31	C31
DATA_BUS[252]	IO_VB3N3_C32	C32
DATA_BUS[253]	IO_VB3N3_C33	C33
DATA_BUS[254]	IO_VB3N3_D31	D31
DATA_BUS[255]	IO_VB3N3_D32	D32
DATA_BUS[256]	IO_VB3N3_D33	D33
DATA_BUS[257]	IO_VB3N3_E29	E29
DATA_BUS[258]	IO_VB3N3_F27	F27
DATA_BUS[259]	IO_VB3N3_G27	G27
DATA_BUS[260]	IO_VB3N3_G28	G28
DATA_BUS[261]	IO_VB3N3_H27	H27
DATA_BUS[262]	IO_VB3N3_J27	J27
DATA_BUS[263]	IO_VB3N3_K27	K27
DATA_BUS[264]	IO_VB3N3_K28	K28
DATA_BUS[265]	IO_VB3N3_L27	L27
DATA_BUS[266]	IO_VB3N3_M26	M26
DATA_BUS[267]	IO_VB3N3_M27	M27
DATA_BUS[268]	IO_VB3N3_N26	N26
DATA_BUS[269]	IO_VB3N3_N27	N27
DATA_BUS[270]	IO_VB3N4_A34	A34
DATA_BUS[271]	IO_VB3N4_A35	A35
DATA_BUS[272]	IO_VB3N4_B34	B34
DATA_BUS[273]	IO_VB3N4_B35	B35
DATA_BUS[274]	IO_VB3N4_C34	C34
DATA_BUS[275]	IO_VB3N4_C35	C35
DATA_BUS[276]	IO_VB3N4_E30	E30

DATA_BUS[277]	IO_VB3N4_F29	F29
DATA_BUS[278]	IO_VB3N4_F30	F30
DATA_BUS[279]	IO_VB3N4_G29	G29
DATA_BUS[280]	IO_VB3N4_H28	H28
DATA_BUS[281]	IO_VB3N4_J28	J28
DATA_BUS[282]	IO_VB3N4_L28	L28
DATA_BUS[283]	IO_VB3N4_M28	M28
DATA_BUS[284]	IO_VB4N0_A5	A5
DATA_BUS[285]	IO_VB4N0_B5	B5
DATA_BUS[286]	IO_VB4N0_B6	B6
DATA_BUS[287]	IO_VB4N0_C5	C5
DATA_BUS[288]	IO_VB4N0_C6	C6
DATA_BUS[289]	IO_VB4N0_D6	D6
DATA_BUS[290]	IO_VB4N0_E9	E9
DATA_BUS[291]	IO_VB4N0_F10	F10
DATA_BUS[292]	IO_VB4N0_F11	F11
DATA_BUS[293]	IO_VB4N0_G11	G11
DATA_BUS[294]	IO_VB4N0_G12	G12
DATA_BUS[295]	IO_VB4N0_H11	H11
DATA_BUS[296]	IO_VB4N0_H12	H12
DATA_BUS[297]	IO_VB4N0_K12	K12
DATA_BUS[298]	IO_VB4N0_K13	K13
DATA_BUS[299]	IO_VB4N0_L13	L13
DATA_BUS[300]	IO_VB4N0_M13	M13
DATA_BUS[301]	IO_VB4N0_M14	M14
DATA_BUS[302]	IO_VB4N0_N13	N13
DATA_BUS[303]	IO_VB4N0_N14	N14
DATA_BUS[304]	IO_VB4N0_N15	N15
DATA_BUS[305]	IO_VB4N0_P15	P15
DATA_BUS[306]	IO_VB4N1_A6	A6
DATA_BUS[307]	IO_VB4N1_A7	A7
DATA_BUS[308]	IO_VB4N1_A8	A8
DATA_BUS[309]	IO_VB4N1_A9	A9
DATA_BUS[310]	IO_VB4N1_B7	B7
DATA_BUS[311]	IO_VB4N1_B8	B8
DATA_BUS[312]	IO_VB4N1_B9	B9
DATA_BUS[313]	IO_VB4N1_C7	C7
DATA_BUS[314]	IO_VB4N1_C8	C8
DATA_BUS[315]	IO_VB4N1_C9	C9
DATA_BUS[316]	IO_VB4N1_C10	C10
DATA_BUS[317]	IO_VB4N1_D7	D7
DATA_BUS[318]	IO_VB4N1_D8	D8
DATA_BUS[319]	IO_VB4N1_D9	D9
DATA_BUS[320]	IO_VB4N1_D10	D10
DATA_BUS[321]	IO_VB4N1_E10	E10
DATA_BUS[322]	IO_VB4N1_G13	G13
DATA_BUS[323]	IO_VB4N1_G14	G14
DATA_BUS[324]	IO_VB4N1_G15	G15
DATA_BUS[325]	IO_VB4N1_H13	H13
DATA_BUS[326]	IO_VB4N1_H14	H14
DATA_BUS[327]	IO_VB4N1_J12	J12

DATA_BUS[328]	IO_VB4N1_J13	J13
DATA_BUS[329]	IO_VB4N1_K14	K14
DATA_BUS[330]	IO_VB4N1_L14	L14
DATA_BUS[331]	IO_VB4N1_L15	L15
DATA_BUS[332]	IO_VB4N1_M15	M15
DATA_BUS[333]	IO_VB4N1_M16	M16
DATA_BUS[334]	IO_VB4N1_N16	N16
DATA_BUS[335]	IO_VB4N2_A10	A10
DATA_BUS[336]	IO_VB4N2_A11	A11
DATA_BUS[337]	IO_VB4N2_A12	A12
DATA_BUS[338]	IO_VB4N2_A13	A13
DATA_BUS[339]	IO_VB4N2_B10	B10
DATA_BUS[340]	IO_VB4N2_B11	B11
DATA_BUS[341]	IO_VB4N2_B12	B12
DATA_BUS[342]	IO_VB4N2_B13	B13
DATA_BUS[343]	IO_VB4N2_C11	C11
DATA_BUS[344]	IO_VB4N2_C12	C12
DATA_BUS[345]	IO_VB4N2_D11	D11
DATA_BUS[346]	IO_VB4N2_D12	D12
DATA_BUS[347]	IO_VB4N2_E11	E11
DATA_BUS[348]	IO_VB4N2_E12	E12
DATA_BUS[349]	IO_VB4N2_G16	G16
DATA_BUS[350]	IO_VB4N2_G17	G17
DATA_BUS[351]	IO_VB4N2_G18	G18
DATA_BUS[352]	IO_VB4N2_H15	H15
DATA_BUS[353]	IO_VB4N2_H16	H16
DATA_BUS[354]	IO_VB4N2_J14	J14
DATA_BUS[355]	IO_VB4N2_J15	J15
DATA_BUS[356]	IO_VB4N2_K15	K15
DATA_BUS[357]	IO_VB4N2_K16	K16
DATA_BUS[358]	IO_VB4N2_L16	L16
DATA_BUS[359]	IO_VB4N2_L17	L17
DATA_BUS[360]	IO_VB4N2_M17	M17
DATA_BUS[361]	IO_VB4N2_M18	M18
DATA_BUS[362]	IO_VB4N2_N17	N17
DATA_BUS[363]	IO_VB4N2_N18	N18
DATA_BUS[364]	IO_VB4N3_A14	A14
DATA_BUS[365]	IO_VB4N3_A15	A15
DATA_BUS[366]	IO_VB4N3_B14	B14
DATA_BUS[367]	IO_VB4N3_B15	B15
DATA_BUS[368]	IO_VB4N3_C13	C13
DATA_BUS[369]	IO_VB4N3_C14	C14
DATA_BUS[370]	IO_VB4N3_C15	C15
DATA_BUS[371]	IO_VB4N3_D13	D13
DATA_BUS[372]	IO_VB4N3_D14	D14
DATA_BUS[373]	IO_VB4N3_D15	D15
DATA_BUS[374]	IO_VB4N3_E13	E13
DATA_BUS[375]	IO_VB4N3_E14	E14
DATA_BUS[376]	IO_VB4N3_E15	E15
DATA_BUS[377]	IO_VB4N3_F13	F13
DATA_BUS[378]	IO_VB6N2_AD12	AD12

DATA_BUS[379]	IO_VB6N1_AF12	AF12
DATA_BUS[380]	IO_VB6N3_AF1	AF1
DATA_BUS[381]	IO_VB6N3_AF2	AF2
DATA_BUS[382]	IO_VB6N1_AG13	AG13
DATA_BUS[383]	IO_VB6N2_AG3	AG3
DATA_BUS[384]	IO_VB6N1_AH10	AH10
DATA_BUS[385]	IO_VB6N1_AH11	AH11
DATA_BUS[386]	IO_VB6N0_AJ7	AJ7
DATA_BUS[387]	IO_VB6N3_AH2	AH2
DATA_BUS[388]	IO_VB6N3_AJ2	AJ2
DATA_BUS[389]	IO_VB6N0_AK8	AK8
DATA_BUS[390]	IO_VB6N1_AL5	AL5
DATA_BUS[391]	IO_VB6N2_AM2	AM2
DATA_BUS[392]	IO_VB6N0_AN6	AN6
DATA_BUS[393]	IO_VB6N0_AR3	AR3
DATA_BUS[394]	IO_VB6N4_AC1	AC1
DATA_BUS[395]	IO_VB6N4_AC2	AC2
DATA_BUS[396]	IO_VB6N3_AD4	AD4
DATA_BUS[397]	IO_VB6N1_AE14	AE14
DATA_BUS[398]	IO_VB6N2_AE11	AE11
DATA_BUS[399]	IO_VB6N1_AF13	AF13
DATA_BUS[400]	IO_VB6N2_AF5	AF5
DATA_BUS[401]	IO_VB6N3_AF3	AF3
DATA_BUS[402]	IO_VB6N2_AG4	AG4
DATA_BUS[403]	IO_VB6N1_AH12	AH12
DATA_BUS[404]	IO_VB6N2_AH3	AH3
DATA_BUS[405]	IO_VB6N0_AJ8	AJ8
DATA_BUS[406]	IO_VB6N0_AJ9	AJ9
DATA_BUS[407]	IO_VB6N0_AK9	AK9
DATA_BUS[408]	IO_VB6N1_AK5	AK5
DATA_BUS[409]	IO_VB6N1_AK6	AK6
DATA_BUS[410]	IO_VB6N1_AL6	AL6
DATA_BUS[411]	IO_VB6N2_AL1	AL1
DATA_BUS[412]	IO_VB6N2_AL2	AL2
DATA_BUS[413]	IO_VB6N2_AL3	AL3
DATA_BUS[414]	IO_VB6N0_AN7	AN7
DATA_BUS[415]	IO_VB6N1_AN1	AN1
DATA_BUS[416]	IO_VB6N1_AN2	AN2
DATA_BUS[417]	IO_VB6N0_AR4	AR4
DATA_BUS[418]	IO_VB6N0_AR5	AR5
DATA_BUS[419]	IO_VB6N0_AR6	AR6
DATA_BUS[420]	IO_VB6N1_AD13	AD13
DATA_BUS[421]	IO_VB6N1_AD14	AD14
DATA_BUS[422]	IO_VB6N3_AD5	AD5
DATA_BUS[423]	IO_VB6N3_AD8	AD8
DATA_BUS[424]	IO_VB6N2_AE5	AE5
DATA_BUS[425]	IO_VB6N2_AE6	AE6
DATA_BUS[426]	IO_VB6N2_AE12	AE12
DATA_BUS[427]	IO_VB6N3_AE3	AE3
DATA_BUS[428]	IO_VB6N2_AF6	AF6
DATA_BUS[429]	IO_VB6N2_AF7	AF7

DATA_BUS[430]	IO_VB6N3_AF4	AF4
DATA_BUS[431]	IO_VB6N1_AG8	AG8
DATA_BUS[432]	IO_VB6N2_AG6	AG6
DATA_BUS[433]	IO_VB6N2_AG7	AG7
DATA_BUS[434]	IO_VB6N2_AH4	AH4
DATA_BUS[435]	IO_VB6N0_AJ10	AJ10
DATA_BUS[436]	IO_VB6N1_AJ5	AJ5
DATA_BUS[437]	IO_VB6N1_AJ6	AJ6
DATA_BUS[438]	IO_VB6N2_AK3	AK3
DATA_BUS[439]	IO_VB6N2_AK4	AK4
DATA_BUS[440]	IO_VB6N2_AL4	AL4
DATA_BUS[441]	IO_VB6N0_AM5	AM5
DATA_BUS[442]	IO_VB6N1_AN3	AN3
DATA_BUS[443]	IO_VB6N1_AN4	AN4
DATA_BUS[444]	IO_VB6N0_AP3	AP3
DATA_BUS[445]	IO_VB6N1_AR1	AR1
DATA_BUS[446]	IO_VB6N1_AR2	AR2
DATA_BUS[447]	IO_VB6N0_AT3	AT3
DATA_BUS[448]	IO_VB6N2_AD6	AD6
DATA_BUS[449]	IO_VB6N2_AD7	AD7
DATA_BUS[450]	IO_VB6N3_AD9	AD9
DATA_BUS[451]	IO_VB6N4_AD2	AD2
DATA_BUS[452]	IO_VB6N4_AD3	AD3
DATA_BUS[453]	IO_VB6N2_AE7	AE7
DATA_BUS[454]	IO_VB6N2_AE8	AE8
DATA_BUS[455]	IO_VB6N3_AE4	AE4
DATA_BUS[456]	IO_VB6N4_AE1	AE1
DATA_BUS[457]	IO_VB6N2_AF8	AF8
DATA_BUS[458]	IO_VB6N1_AG9	AG9
DATA_BUS[459]	IO_VB6N1_AG10	AG10
DATA_BUS[460]	IO_VB6N3_AG1	AG1
DATA_BUS[461]	IO_VB6N2_AJ3	AJ3
DATA_BUS[462]	IO_VB6N2_AJ4	AJ4
DATA_BUS[463]	IO_VB6N3_AK1	AK1
DATA_BUS[464]	IO_VB6N3_AK2	AK2
DATA_BUS[465]	IO_VB6N0_AL8	AL8
DATA_BUS[466]	IO_VB6N0_AL9	AL9
DATA_BUS[467]	IO_VB6N0_AM6	AM6
DATA_BUS[468]	IO_VB6N0_AM8	AM8
DATA_BUS[469]	IO_VB6N0_AM9	AM9
DATA_BUS[470]	IO_VB6N1_AM3	AM3
DATA_BUS[471]	IO_VB6N0_AP4	AP4
DATA_BUS[472]	IO_VB6N0_AP5	AP5
DATA_BUS[473]	IO_VB6N0_AP6	AP6
DATA_BUS[474]	IO_VB6N0_AT4	AT4
DATA_BUS[475]	IO_VB6N0_AU3	AU3
DATA_BUS[476]	IO_VB6N0_AU4	AU4
DATA_BUS[477]	IO_VB6N2_AD11	AD11
DATA_BUS[478]	IO_VB6N1_AE13	AE13
DATA_BUS[479]	IO_VB6N2_AE9	AE9
DATA_BUS[480]	IO_VB6N2_AE10	AE10

DATA_BUS[481]	IO_VB6N4_AE2	AE2
DATA_BUS[482]	IO_VB6N2_AF10	AF10
DATA_BUS[483]	IO_VB6N1_AG11	AG11
DATA_BUS[484]	IO_VB6N1_AG12	AG12
DATA_BUS[485]	IO_VB6N3_AG2	AG2
DATA_BUS[486]	IO_VB6N1_AH7	AH7
DATA_BUS[487]	IO_VB6N1_AH8	AH8
DATA_BUS[488]	IO_VB6N2_AH5	AH5
DATA_BUS[489]	IO_VB6N2_AH6	AH6
DATA_BUS[490]	IO_VB6N3_AH1	AH1
DATA_BUS[491]	IO_VB6N3_AJ1	AJ1
DATA_BUS[492]	IO_VB6N1_AM4	AM4
DATA_BUS[493]	IO_VB6N2_AM1	AM1
DATA_BUS[494]	IO_VB6N1_AP1	AP1
DATA_BUS[495]	IO_VB6N1_AP2	AP2
DATA_BUS[496]	IO_VB6N1_AV2	AV2
DATA_BUS[497]	IO_VB6N1_AV3	AV3
DATA_BUS[498]	IO_VB6N2_AF11	AF11
DATA_BUS[499]	IO_VB6N1_AH9	AH9
DATA_BUS[500]	IO_VB6N4_Y5	Y5
DATA_BUS[501]	IO_VB6N4_Y6	Y6
DATA_BUS[502]	PLL6_OUT0n	AV19
DATA_BUS[503]	PLL6_OUT0p	AW19
DATA_BUS[504]	PLL6_OUT1n	AU18
DATA_BUS[505]	PLL6_OUT1p	AV18
DATA_BUS[506]	PLL6_FBn	AR18
DATA_BUS[507]	PLL6_FBp	AT18
DATA_BUS[508]	CLK13n	D19
DATA_BUS[509]	CLK13p	C19
DATA_BUS[510]	CLK14n	D21
DATA_BUS[511]	CLK14p	C21

Table 8.1: 512-bit bus connection to the *DUT-FPGA#1*.

The signal *DATA_BUS[509]* is connected to the clock input pin 13. The signal *DATA_BUS[511]* is connected to the clock input pin 14. The signals *DATA_BUS[503]*, *DATA_BUS[505]* and *DATA_BUS[507]* are connected to the PLL output pins of PLL 5.

8.2.1 LVDS connection to DUT-FPGA#1

Differential Transmit Channels

The signals in table 8.2 show the transmiter pairs for the LVDS connection to the *DUT-FPGA#1*.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
RX1_TX2-[0]	IO_VB1N0_AA30	AA30
RX1_TX2-[1]	IO_VB1N0_AA28	AA28
RX1_TX2-[2]	IO_VB1N0_Y32	Y32
RX1_TX2-[3]	IO_VB1N0_AA32	AA32
RX1_TX2-[4]	IO_VB1N0_Y34	Y34

RX1_TX2-[5]	IO_VB1N0_AB29	AB29
RX1_TX2-[6]	IO_VB1N0_AA26	AA26
RX1_TX2-[7]	IO_VB1N1_AB31	AB31
RX1_TX2-[8]	IO_VB1N1_AB33	AB33
RX1_TX2-[9]	IO_VB1N1_AB27	AB27
RX1_TX2-[10]	IO_VB1N1_AC29	AC29
RX1_TX2-[11]	IO_VB1N1_AC27	AC27
RX1_TX2-[12]	IO_VB1N1_AC31	AC31
RX1_TX2-[13]	IO_VB1N1_AC33	AC33
RX1_TX2-[14]	IO_VB1N1_AD31	AD31
RX1_TX2-[15]	IO_VB1N1_AD33	AD33
RX1_TX2-[16]	IO_VB2N4_Y26	Y26
RX1_TX2-[17]	IO_VB2N4_W27	W27
RX1_TX2-[18]	IO_VB2N4_W32	W32
RX1_TX2-[19]	IO_VB2N4_V33	V33
RX1_TX2-[20]	IO_VB2N4_V31	V31
RX1_TX2-[21]	IO_VB2N4_V27	V27
RX1_TX2-[22]	IO_VB2N4_U27	U27
RX1_TX2-[23]	IO_VB2N4_U33	U33
RX1_TX2-[24]	IO_VB2N3_U29	U29
RX1_TX2-[25]	IO_VB2N3_U31	U31
RX1_TX2-[26]	IO_VB2N3_T27	T27
RX1_TX2-[27]	IO_VB2N3_T33	T33
RX1_TX2-[28]	IO_VB2N3_R33	R33
RX1_TX2-[29]	IO_VB2N3_T31	T31
RX1_TX2-[30]	IO_VB2N3_T29	T29
RX1_TX2-[31]	IO_VB2N3_P34	P34
RX1_TX2+[0]	IO_VB1N0_AA31	AA31
RX1_TX2+[1]	IO_VB1N0_AA29	AA29
RX1_TX2+[2]	IO_VB1N0_Y33	Y33
RX1_TX2+[3]	IO_VB1N0_AA33	AA33
RX1_TX2+[4]	IO_VB1N0_Y35	Y35
RX1_TX2+[5]	IO_VB1N0_AB30	AB30
RX1_TX2+[6]	IO_VB1N0_AA27	AA27
RX1_TX2+[7]	IO_VB1N1_AB32	AB32
RX1_TX2+[8]	IO_VB1N1_AB34	AB34
RX1_TX2+[9]	IO_VB1N1_AB28	AB28
RX1_TX2+[10]	IO_VB1N1_AC30	AC30
RX1_TX2+[11]	IO_VB1N1_AC28	AC28
RX1_TX2+[12]	IO_VB1N1_AC32	AC32
RX1_TX2+[13]	IO_VB1N1_AC34	AC34
RX1_TX2+[14]	IO_VB1N1_AD32	AD32
RX1_TX2+[15]	IO_VB1N1_AD34	AD34
RX1_TX2+[16]	IO_VB2N4_Y27	Y27
RX1_TX2+[17]	IO_VB2N4_W28	W28
RX1_TX2+[18]	IO_VB2N4_W33	W33
RX1_TX2+[19]	IO_VB2N4_V34	V34
RX1_TX2+[20]	IO_VB2N4_V32	V32
RX1_TX2+[21]	IO_VB2N4_V28	V28
RX1_TX2+[22]	IO_VB2N4_U28	U28
RX1_TX2+[23]	IO_VB2N4_U34	U34

RX1_TX2+[24]	IO_VB2N3_U30	U30
RX1_TX2+[25]	IO_VB2N3_U32	U32
RX1_TX2+[26]	IO_VB2N3_T28	T28
RX1_TX2+[27]	IO_VB2N3_T34	T34
RX1_TX2+[28]	IO_VB2N3_R34	R34
RX1_TX2+[29]	IO_VB2N3_T32	T32
RX1_TX2+[30]	IO_VB2N3_T30	T30
RX1_TX2+[31]	IO_VB2N3_P35	P35

Table 8.2: LVDS connection to the *DUT-FPGA#1*: Transmit channels.

Differential Receive Channels

The signals in table 8.3 show the receiver pairs for the LVDS connection to the *DUT-FPGA#1*.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
TX1_RX2-[0]	CLK2n	Y38
TX1_RX2-[1]	IO_VB1N0_AA38	AA38
TX1_RX2-[2]	IO_VB1N0_AA36	AA36
TX1_RX2-[3]	IO_VB1N0_AB37	AB37
TX1_RX2-[4]	IO_VB1N0_AC38	AC38
TX1_RX2-[5]	IO_VB1N0_AB35	AB35
TX1_RX2-[6]	IO_VB1N0_AE38	AE38
TX1_RX2-[7]	IO_VB1N0_AD37	AD37
TX1_RX2-[8]	IO_VB1N1_AC36	AC36
TX1_RX2-[9]	IO_VB1N1_AE36	AE36
TX1_RX2-[10]	IO_VB1N1_AD35	AD35
TX1_RX2-[11]	IO_VB1N1_AF38	AF38
TX1_RX2-[12]	IO_VB1N1_AG38	AG38
TX1_RX2-[13]	IO_VB1N1_AH38	AH38
TX1_RX2-[14]	IO_VB1N1_AF36	AF36
TX1_RX2-[15]	IO_VB1N1_AJ38	AJ38
TX1_RX2-[16]	CLK0n	W38
TX1_RX2-[17]	IO_VB2N4_U38	U38
TX1_RX2-[18]	IO_VB2N4_V37	V37
TX1_RX2-[19]	IO_VB2N4_R38	R38
TX1_RX2-[20]	IO_VB2N4_T37	T37
TX1_RX2-[21]	IO_VB2N4_V35	V35
TX1_RX2-[22]	IO_VB2N4_U36	U36
TX1_RX2-[23]	IO_VB2N4_P38	P38
TX1_RX2-[24]	IO_VB2N4_P36	P36
TX1_RX2-[25]	IO_VB2N3_R36	R36
TX1_RX2-[26]	IO_VB2N3_T35	T35
TX1_RX2-[27]	IO_VB2N3_N38	N38
TX1_RX2-[28]	IO_VB2N3_M38	M38
TX1_RX2-[29]	IO_VB2N3_L38	L38
TX1_RX2-[30]	IO_VB2N3_K38	K38
TX1_RX2-[31]	IO_VB2N3_N36	N36
TX1_RX2+[0]	CLK2p	Y39

TX1_RX2+[1]	IO_VB1N0_AA39	AA39
TX1_RX2+[2]	IO_VB1N0_AA37	AA37
TX1_RX2+[3]	IO_VB1N0_AB38	AB38
TX1_RX2+[4]	IO_VB1N0_AC39	AC39
TX1_RX2+[5]	IO_VB1N0_AB36	AB36
TX1_RX2+[6]	IO_VB1N0_AE39	AE39
TX1_RX2+[7]	IO_VB1N0_AD38	AD38
TX1_RX2+[8]	IO_VB1N1_AC37	AC37
TX1_RX2+[9]	IO_VB1N1_AE37	AE37
TX1_RX2+[10]	IO_VB1N1_AD36	AD36
TX1_RX2+[11]	IO_VB1N1_AF39	AF39
TX1_RX2+[12]	IO_VB1N1_AG39	AG39
TX1_RX2+[13]	IO_VB1N1_AH39	AH39
TX1_RX2+[14]	IO_VB1N1_AF37	AF37
TX1_RX2+[15]	IO_VB1N1_AJ39	AJ39
TX1_RX2+[16]	CLK0p	W39
TX1_RX2+[17]	IO_VB2N4_U39	U39
TX1_RX2+[18]	IO_VB2N4_V38	V38
TX1_RX2+[19]	IO_VB2N4_R39	R39
TX1_RX2+[20]	IO_VB2N4_T38	T38
TX1_RX2+[21]	IO_VB2N4_V36	V36
TX1_RX2+[22]	IO_VB2N4_U37	U37
TX1_RX2+[23]	IO_VB2N4_P39	P39
TX1_RX2+[24]	IO_VB2N4_P37	P37
TX1_RX2+[25]	IO_VB2N3_R37	R37
TX1_RX2+[26]	IO_VB2N3_T36	T36
TX1_RX2+[27]	IO_VB2N3_N39	N39
TX1_RX2+[28]	IO_VB2N3_M39	M39
TX1_RX2+[29]	IO_VB2N3_L39	L39
TX1_RX2+[30]	IO_VB2N3_K39	K39
TX1_RX2+[31]	IO_VB2N3_N37	N37

Table 8.3: LVDS connection to the *DUT-FPGA#1*: Receive channels.

The differential signals *TX1_RX2[0]* are connected to the differential clock input pins 2. The differential signals *TX1_RX2[16]* are connected to the differential clock input pins 0.

8.3 Connection to the CPLD for Clock Factory and Configuration

8.3.1 Configuration Pins for the DUT-FPGA#2 by the CPLD for Clock Factory and Configuration

The signals in table 8.4 can also be reached by the *Hpe_childboard* 1. Only the signals *CB1_DATA[0]* to *CB1_DATA[7]* can be used as normal I/O pins. The others are only for configuration (refer to section 3.2).

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
CB1_CONFIG#	nCONFIG	AM30
CB1_CONF_DONE	CONF_DONE	F33

CB1_DATA[0]	DATA0	H22
CB1_DATA[1]	DATA1	F21
CB1_DATA[2]	DATA2	E31
CB1_DATA[3]	DATA3	E33
CB1_DATA[4]	DATA4	H29
CB1_DATA[5]	DATA5	J29
CB1_DATA[6]	DATA6	E32
CB1_DATA[7]	DATA7	F32
CB1_DCLK	DCLK	D34
CB1_STATUS#	nSTATUS	A37

Table 8.4: Pin connection to the *Hpe_childboard* 1 connector: Configuration pins for the two DUT-FPGAs.

8.3.2 Clocks

The signals in table 8.5 are input clocks driven by the *Clock Factory*. For further details see section 3.1.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
DUT2_CLK3P	CLK3p	Y37
DUT2_CLK4P	CLK4p	AU20
DUT2_CLK5P	CLK5p	AU21
DUT2_CLK6P	CLK6p	AW20
DUT2_CLK7-	CLK7n	AT19
DUT2_CLK7+	CLK7p	AU19
DUT2_CLK8P	CLK8p	Y1
DUT2_CLK9P	CLK9p	Y3
DUT2_CLK12P	CLK12p	A20
DUT2_CLK15-	CLK15n	D20
DUT2_CLK15+	CLK15p	C20

Table 8.5: Clocks from the *Clock Factory*.

The differential clocks *DUT1_CLK7** and *DUT1_CLK15** are delivered in *LVPECL* standard. The pins *DUT1_CLK7-* and *DUT1_CLK15-* are not connected to the *Clock Factory* but only used for the inverted clock signal. All other clocks are driven in normal single ended standard.

8.3.3 I/O Pins: Negative Clock Inputs

The signals in table 8.6 are the negative clock input pins. Since the *Clock Factory* is not able to drive diffential clocks, these pins can be used as normal I/O pins between the *DUT-FPGA#2* and the *Clock Factory*.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
DUT2_CLK1N	CLK1n	W36
DUT2_CLK3N	CLK3n	Y36
DUT2_CLK4N	CLK4n	AT20
DUT2_CLK5N	CLK5n	AT21

DUT2_CLK6N	CLK6n	AV20
DUT2_CLK8N	CLK8n	Y2
DUT2_CLK9N	CLK9n	Y4
DUT2_CLK11N	CLK11n	W4
DUT2_CLK12N	CLK12n	B20

Table 8.6: Negative clock inputs from *Clock Factory*. This signals can be used as normal I/O pins.

8.3.4 Fast PLL Clock Inputs

The signals that end with a *P* in table 8.7 are single ended clock input pins for driving the Fast PLLs in the *DUT-FPGA#2*. Since the *Clock Factory* is not able to drive diffential clocks, the pins that end with an *N* can be used as normal I/O pins between the *DUT-FPGA#2* and the *Clock Factory*.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
DUT2_FPLL7N	FPLL7CLKn	C38
DUT2_FPLL7P	FPLL7CLKp	C39
DUT2_FPLL8N	FPLL8CLKn	AU38
DUT2_FPLL8P	FPLL8CLKp	AU39
DUT2_FPLL9N	FPLL9CLKn	AU2
DUT2_FPLL9P	FPLL9CLKp	AU1
DUT2_FPLL10N	FPLL10CLKn	C2
DUT2_FPLL10P	FPLL10CLKp	C1

Table 8.7: Fast PLL clock inputs. The negative clock inputs can be used as normal I/O pins.

8.3.5 PLL Output Clocks

The signals that end with a *P* in table 8.8 are output clocks which are sent to the *Clock Factory* from where they can be distributed to all input clocks connected to the *Clock Factory*. Although the negative pins (end with an *N*) are connected, they can not be used since the *Clock Factory* is not able to receive differential clocks.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
DUT2_PLL6O0N	PLL5_OUT0n	B19
DUT2_PLL6O0P	PLL5_OUT0p	A19
DUT2_PLL6O1N	PLL5_OUT1n	C18
DUT2_PLL6O1P	PLL5_OUT1p	B18
DUT2_PLL6O2N	PLL5_FBn	E18
DUT2_PLL6O2P	PLL5_FBp	D18
DUT2_PLL11O2N	PLL11_FBn	E22
DUT2_PLL11O2P	PLL11_FBp	D22
DUT2_PLL12O0N	PLL12_OUT0n	AV21
DUT2_PLL12O0P	PLL12_OUT0p	AW21
DUT2_PLL12O1N	PLL12_OUT1n	AU22
DUT2_PLL12O1P	PLL12_OUT1p	AV22

DUT2_PLL12O2N	PLL12_FBn	AR22
DUT2_PLL12O2P	PLL12_FBp	AT22

Table 8.8: PLL output clocks. The negative clock outputs can be used as normal I/O pins.

8.3.6 Other I/O pins

Table 8.9 gives you all other signals connected between *DUT-FPGA#2* and *Clock Factory*.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
DUT2_CLKUSR	CLKUSR	AP30
DUT2_CRC_ERROR	CRC_ERROR	G22
DUT2_CS	CS	AR32
DUT2_CS#	nCS	AP21
DUT2_DEV_OE	DEV_OE	AN20
DUT2_RDY#_BSY	RDYnBSY	G31
DUT2_RSn	nRS	AR30
DUT2_RU#_LU	RUnLU	AM20
DUT2_WS#	nWS	AR31

Table 8.9: All other I/O pins between *DUT-FPGA#2* and *Clock Factory*.

8.4 Connection to the CPLD for USB Blaster and FCP

The signals in table 8.10 are internal signals needed for maintenance. Please do not use them.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
DUT2_INIT_DONE	INIT_DONE	H30
DUT2_PGM[0]	PGM0	G21
DUT2_PGM[1]	PGM1	F20
DUT2_PGM[2]	PGM2	E20

Table 8.10: Pins needed for the FCP.

8.5 Dedicated Pins on the DUT-FPGA#1

8.5.1 Thermal Control

The signals in table 8.11 can not be used as I/O pins. They are needed for the thermal control of the *DUT-FPGA#2*. For more information refer to section 3.3.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
DUT2_TEMPDIODE-	TEMPDIODEn	F7
DUT2_TEMPDIODE+	TEMPDIODEp	B4

Table 8.11: Temperature diode.

8.5.2 JTAG Pins

The signals in table 8.12 are dedicated JTAG pins. They can not be used as I/O pins.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
DUT2_TDI	TDI	AN31
DUT2_TDO	TDO	F8
TCK_DUT	TCK	AP32
TMS_DUT	TMS	AP33
MIDI_TRST	TRST	AW37

Table 8.12: JTAG signals.

8.5.3 Configuration Pins

The signals in table 8.13 can be reached by the *Hpe_childboard* 1 and by the *Clock Factory*. Only the signals *CB1_DATA[0]* to *CB1_DATA[7]* can be used as normal I/O pins, the others are only for configuration. For configuration refer to section 3.2.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
CB1_CONFIG#	nCONFIG	AM30
CB1_CONF_DONE	CONF_DONE	F33
CB1_DATA[0]	DATA0	H22
CB1_DATA[1]	DATA1	F21
CB1_DATA[2]	DATA2	E31
CB1_DATA[3]	DATA3	E33
CB1_DATA[4]	DATA4	H29
CB1_DATA[5]	DATA5	J29
CB1_DATA[6]	DATA6	E32
CB1_DATA[7]	DATA7	F32
CB1_DCLK	DCLK	D34
CB1_STATUS#	nSTATUS	A37

Table 8.13: Pin connection to the *Hpe_childboard* 1 connector: Configuration pins for the *DUT-FPGA#2*.

8.5.4 Other dedicated Configuration Pins

The signals in table 8.14 are other dedicated configuration pins. They can not be used as I/O pins.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
D1_CEO#_D2_CE#	nCE	B36
DUT2_IO_PULLUP#	nIO_PULLUP	AT5
DUT2_MSEL[0]	MSEL0	H10
DUT2_MSEL[1]	MSEL1	G9

DUT2_MSEL[2]	MSEL2	E7
DUT2_MSEL[3]	MSEL3	A3
DUT2_PORSEL	PORSEL	AP7

Table 8.14: Dedicated configuration pins.

- *D1_CEO#_D2_CE#:* Dedicated pin, that ensures that *DUT-FPGA#1* is configured before *DUT-FPGA#2*.
- *DUT2_IO_PULLUP:* Dedicated pin that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins are on or off before and during configuration. These pull-ups are turned on by default.
- *DUT2_MSEL:* Configuration input pins that set the *Altera Stratix II* device configuration scheme. Set to *Fast Passive Parallel* mode by default.
- *DUT2_PORSEL:* Dedicated pin, that selects between a *Power On Reset* time of 12 ms or 100 ms. Set to 12 ms by default.

For further details of these pins refer to the handbook of the *Altera Stratix II*.

8.6 Clock from Oscillator

The 100 MHz clock in table 8.15 is needed for the LVDS connection between the *HMX2-AS2* and the *Communication Controller* on the *HC-PCIe* (which has to be connected to the *Hpe_childboard* 1 connector for *SEmulation* mode).

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
DUT2_CLK100M[1]	CLK11p	W3
DUT2_CLK100M[2]	CLK1p	W37

Table 8.15: 100 MHz clock from an external oscillator.

8.7 Hpe_Childboard 1

In order to be able to use LVDS signaling the *DUT-FPGA#1* requires an I/O supply of 2.5 V on the banks involved. By default these 2.5 V are provided. They are necessary when a *Hpe_childboard* with differential signals is connected to the connector X3. However, when a *Hpe_childboard* without any LVDS signals is connected to X3, then the I/O supply of the concerned banks can be changed to 3.3 V. A low on the signal *CB1_SEL_LVDS_VAL*, controlled by the *Hpe_childboard* 1 switches to 3.3 V. By default this signal is set to high by a pull-up resistor, hence 2.5 V are provided.

For a description of the pins, refer to 5.2.1. All I/O pins of this *Hpe_childboard* that are not connected to the *DUT-FPGA#2*, are connected to *DUT-FPGA#1*.

8.7.1 Differential Receive Channels

The signals in table 8.16 are the differential receiver channels from the *Hpe_childboard* 1.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*	*Childboard connector pin*
CB1_RX_CLK2+	CLK10p	W1	A17
CB1_RX_CLK2-	CLK10n	W2	A19
CB1_RX-[04]	IO_VB5N0_V3	V3	A21
CB1_RX-[05]	IO_VB5N0_U2	U2	A23
CB1_RX-[06]	IO_VB5N0_R2	R2	A25
CB1_RX+[04]	IO_VB5N0_V2	V2	A27
CB1_RX+[05]	IO_VB5N0_U1	U1	A29
CB1_RX+[06]	IO_VB5N0_R1	R1	A31

Table 8.16: Pin connection to the *Hpe_childboard* 1 connector: Receive channels.

The differential signals *CB1_RX_CLK1* are connected to the differential clock input pins 10.

8.7.2 Differential Transmit Channels

The signals in table 8.17 are the differential transmiter channels from the *Hpe_childboard* 1.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*	*Childboard connector pin*
CB1_TX_CLK2+	IO_VB5N0_W7	W7	A18
CB1_TX_CLK2-	IO_VB5N0_W8	W8	A20
CB1_TX-[04]	IO_VB5N0_W13	W13	A22
CB1_TX-[05]	IO_VB5N0_V7	V7	A24
CB1_TX-[06]	IO_VB5N0_V9	V9	A26
CB1_TX+[04]	IO_VB5N0_W12	W12	A28
CB1_TX+[05]	IO_VB5N0_V6	V6	A30
CB1_TX+[06]	IO_VB5N0_V8	V8	A32

Table 8.17: Pin connection to the *Hpe_childboard* 1 connector: Transmit channels

8.7.3 Configuration Pins for the DUT-FPGA#1 by the Hpe_Childboard 1

The signals in table 8.18 can also be reached by the *Clock Factory*. Only the signals *CB1_DATA[0]* to *CB1_DATA[7]* can be used as normal I/O pins. The others are only for configuration.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*	*Childboard connector pin*
CB1_CONFIG#	nCONFIG	AM30	A62
CB1_CONF_DONE	CONF_DONE	F33	A56
CB1_DATA[0]	DATA0	H22	A53
CB1_DATA[1]	DATA1	F21	A55
CB1_DATA[2]	DATA2	E31	A57
CB1_DATA[3]	DATA3	E33	A59
CB1_DATA[4]	DATA4	H29	A61
CB1_DATA[5]	DATA5	J29	A63
CB1_DATA[6]	DATA6	E32	A65
CB1_DATA[7]	DATA7	F32	A54
CB1_DCLK	DCLK	D34	A60
CB1_STATUS#	nSTATUS	A37	A58

Table 8.18: Pin connection to the *Hpe_childboard* 1 connector: Configuration pins for the two DUT-FPGAs.

8.7.4 Other pins to DUT#2

Table 8.19 gives you an overview of all other signals connected to the *Hpe_childboard* 1.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*	*Childboard connector pin*
CB1_RFU[2]	IO_VB5N1_H1	H1	B66

Table 8.19: Pin connection to the *Hpe_childboard* 1 connector: Other pins

The signal *CB1_RFU[2]* works as a reset for the differential transceiver.

8.8 Connector to the Mainboard

The following description is based on the presumption that the *Hpe_midi* is used as a mainboard. For a detailed description of the pins, refer to the manual of the *Hpe_midi*.

8.8.1 Hpe_Childboard 3

Table 8.20 lists all signals connected to this *Hpe_childboard* on the mainboard.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*	*Childboard connector pin*
CB3_CLK+	PLL11_OUT0p	A21	A49
CB3_CLK-	PLL11_OUT0n	B21	A50
CB3_DATA[0]	IO_VB7N1_AG19	AG19	A1
CB3_DATA[1]	IO_VB7N1_AG20	AG20	A2
CB3_DATA[2]	IO_VB7N4_AW5	AW5	B1
CB3_DATA[3]	IO_VB7N4_AW6	AW6	B2
CB3_DATA[4]	IO_VB7N3_AW9	AW9	A3
CB3_DATA[5]	IO_VB7N4_AG14	AG14	A4
CB3_DATA[6]	IO_VB7N1_AU13	AU13	B3
CB3_DATA[7]	IO_VB7N3_AW7	AW7	B4
CB3_DATA[8]	IO_VB7N3_AW8	AW8	A5
CB3_DATA[9]	IO_VB7N1_AU14	AU14	A6
CB3_DATA[10]	IO_VB7N2_AW10	AW10	B5
CB3_DATA[11]	IO_VB7N2_AW11	AW11	B6
CB3_DATA[12]	IO_VB7N2_AW12	AW12	A7
CB3_DATA[13]	IO_VB7N4_AV5	AV5	A8
CB3_DATA[14]	IO_VB7N4_AV6	AV6	B7
CB3_DATA[15]	IO_VB7N3_AV7	AV7	B8
CB3_DATA[16]	IO_VB7N3_AV8	AV8	A9
CB3_DATA[17]	IO_VB7N3_AV9	AV9	A10
CB3_DATA[18]	IO_VB7N2_AV10	AV10	B9
CB3_DATA[19]	IO_VB7N2_AV11	AV11	B10
CB3_DATA[20]	IO_VB7N2_AT12	AT12	A11

CB3_DATA[21]	IO_VB7N3_AG16	AG16	A12
CB3_DATA[22]	IO_VB7N2_AG17	AG17	B11
CB3_DATA[23]	IO_VB7N2_AG18	AG18	B12
CB3_DATA[24]	IO_VB7N4_AH13	AH13	A13
CB3_DATA[25]	IO_VB7N3_AH14	AH14	A14
CB3_DATA[26]	IO_VB7N0_AH20	AH20	B13
CB3_DATA[27]	IO_VB7N2_AV12	AV12	B14
CB3_DATA[28]	IO_VB7N4_AU5	AU5	A15
CB3_DATA[29]	IO_VB7N4_AU6	AU6	A16
CB3_DATA[30]	IO_VB7N3_AU10	AU10	B15
CB3_DATA[31]	IO_VB7N1_AH19	AH19	B16
CB3_DATA[32]	IO_VB7N2_AH17	AH17	A17
CB3_DATA[33]	IO_VB7N2_AH18	AH18	A18
CB3_DATA[34]	IO_VB7N3_AH15	AH15	B17
CB3_DATA[35]	IO_VB7N3_AH16	AH16	B18
CB3_DATA[36]	IO_VB7N1_AJ18	AJ18	A19
CB3_DATA[37]	IO_VB7N2_AJ16	AJ16	A20
CB3_DATA[38]	IO_VB7N2_AJ17	AJ17	B19
CB3_DATA[39]	IO_VB7N3_AJ14	AJ14	B20
CB3_DATA[40]	IO_VB7N3_AJ15	AJ15	A21
CB3_DATA[41]	IO_VB7N1_AK17	AK17	A22
CB3_DATA[42]	IO_VB7N2_AK15	AK15	B21
CB3_DATA[43]	IO_VB7N4_AJ12	AJ12	B22
CB3_DATA[44]	IO_VB7N3_AK13	AK13	A23
CB3_DATA[45]	IO_VB7N3_AK14	AK14	A24
CB3_DATA[46]	IO_VB7N2_AK16	AK16	B23
CB3_DATA[47]	IO_VB7N3_AU7	AU7	B24
CB3_DATA[48]	IO_VB7N3_AU8	AU8	A25
CB3_DATA[49]	IO_VB7N3_AU9	AU9	A26
CB3_DATA[50]	IO_VB7N2_AU11	AU11	B25
CB3_DATA[51]	IO_VB7N2_AU12	AU12	B26
CB3_DATA[52]	IO_VB7N3_AT7	AT7	A27
CB3_DATA[53]	IO_VB7N3_AT8	AT8	A28
CB3_DATA[54]	IO_VB7N3_AT9	AT9	B27
CB3_DATA[55]	IO_VB7N3_AT10	AT10	B28
CB3_DATA[56]	IO_VB7N1_AU15	AU15	A29
CB3_DATA[57]	IO_VB7N1_AU16	AU16	A30
CB3_DATA[58]	IO_VB7N0_AU17	AU17	B29
CB3_DATA[59]	IO_VB7N1_AV13	AV13	B30
CB3_DATA[60]	IO_VB7N1_AV14	AV14	A31
CB3_DATA[61]	IO_VB7N1_AV15	AV15	A32
CB3_DATA[62]	IO_VB7N0_AV16	AV16	B31
CB3_DATA[63]	IO_VB7N0_AV17	AV17	B32
CB3_DATA[64]	IO_VB7N1_AW13	AW13	B34
CB3_DATA[65]	IO_VB7N1_AW14	AW14	B49
CB3_DATA[66]	IO_VB7N1_AW15	AW15	B50
CB3_DATA[67]	IO_VB7N0_AW17	AW17	B51
CB3_DATA[68]	IO_VB7N3_AL13	AL13	B52
CB3_DATA[69]	IO_VB7N2_AL14	AL14	A53
CB3_DATA[70]	IO_VB7N2_AL15	AL15	A54
CB3_DATA[71]	IO_VB7N4_AM11	AM11	B53

CB3_DATA[72]	IO_VB7N4_AM12	AM12	B54
CB3_DATA[73]	IO_VB7N3_AM13	AM13	A55
CB3_DATA[74]	IO_VB7N3_AM14	AM14	A56
CB3_DATA[75]	IO_VB7N2_AM15	AM15	B55
CB3_DATA[76]	IO_VB7N2_AM16	AM16	B56
CB3_DATA[77]	IO_VB7N4_AN11	AN11	A57
CB3_DATA[78]	IO_VB7N4_AN12	AN12	A58
CB3_DATA[79]	IO_VB7N4_AN13	AN13	B57
CB3_DATA[80]	IO_VB7N0_AL18	AL18	B58
CB3_DATA[81]	IO_VB7N1_AL16	AL16	A59
CB3_DATA[82]	IO_VB7N1_AL17	AL17	A60
CB3_DATA[83]	IO_VB7N0_AM18	AM18	B59
CB3_DATA[84]	IO_VB7N0_AM19	AM19	B60
CB3_DATA[85]	IO_VB7N1_AM17	AM17	A61
CB3_DATA[86]	IO_VB7N0_AN18	AN18	A62
CB3_DATA[87]	IO_VB7N0_AN19	AN19	B61
CB3_DATA[88]	IO_VB7N1_AN17	AN17	B62
CB3_DATA[89]	IO_VB7N2_AN15	AN15	A63
CB3_DATA[90]	IO_VB7N2_AN16	AN16	A64
CB3_DATA[91]	IO_VB7N0_AP16	AP16	B63
CB3_DATA[92]	IO_VB7N0_AP19	AP19	B64
CB3_DATA[93]	IO_VB7N1_AP14	AP14	A65
CB3_DATA[94]	IO_VB7N4_AJ13	AJ13	A66
CB3_DATA[95]	IO_VB7N4_AK12	AK12	B65
CB3_DATA[96]	IO_VB7N4_AL12	AL12	B66

Table 8.20: Pin connection to the module connector: *Hpe_childboard* 3 connector.

The differential signals *CB3_CLK** are connected to PLL output pins of the PLL 11.

8.8.2 Hpe_Childboard 4

Table 8.21 lists all signals connected to this *Hpe_childboard* on the mainboard.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*	*Childboard connector pin*
CB4_CLK+	PLL11_OUT1p	B22	A49
CB4_CLK-	PLL11_OUT1n	C22	A50
CB4_DATA[0]	IO_VB8N2_AV28	AV28	A1
CB4_DATA[1]	IO_VB8N2_AV29	AV29	A2
CB4_DATA[2]	IO_VB8N2_AV30	AV30	B1
CB4_DATA[3]	IO_VB8N1_AU31	AU31	B2
CB4_DATA[4]	IO_VB8N1_AU32	AU32	A3
CB4_DATA[5]	IO_VB8N1_AU33	AU33	A4
CB4_DATA[6]	IO_VB8N1_AW31	AW31	B3
CB4_DATA[7]	IO_VB8N0_AW34	AW34	B4
CB4_DATA[8]	IO_VB8N3_AV27	AV27	A5
CB4_DATA[9]	IO_VB8N3_AW25	AW25	A6
CB4_DATA[10]	IO_VB8N3_AW26	AW26	B5
CB4_DATA[11]	IO_VB8N2_AW28	AW28	B6
CB4_DATA[12]	IO_VB8N2_AW29	AW29	A7

CB4_DATA[13]	IO_VB8N2_AW30	AW30	A8
CB4_DATA[14]	IO_VB8N1_AV31	AV31	B7
CB4_DATA[15]	IO_VB8N1_AV32	AV32	B8
CB4_DATA[16]	IO_VB8N1_AV33	AV33	A9
CB4_DATA[17]	IO_VB8N1_AW32	AW32	A10
CB4_DATA[18]	IO_VB8N1_AW33	AW33	B9
CB4_DATA[19]	IO_VB8N3_AW27	AW27	B10
CB4_DATA[20]	IO_VB8N2_AT29	AT29	A11
CB4_DATA[21]	IO_VB8N2_AT30	AT30	A12
CB4_DATA[22]	IO_VB8N1_AT31	AT31	B11
CB4_DATA[23]	IO_VB8N1_AT32	AT32	B12
CB4_DATA[24]	IO_VB8N1_AT33	AT33	A13
CB4_DATA[25]	IO_VB8N0_AW35	AW35	A14
CB4_DATA[26]	IO_VB8N0_AV34	AV34	B13
CB4_DATA[27]	IO_VB8N0_AV35	AV35	B14
CB4_DATA[28]	IO_VB8N0_AU34	AU34	A15
CB4_DATA[29]	IO_VB8N0_AU35	AU35	A16
CB4_DATA[30]	IO_VB8N4_AG21	AG21	B15
CB4_DATA[31]	IO_VB8N3_AG22	AG22	B16
CB4_DATA[32]	IO_VB8N3_AG23	AG23	A17
CB4_DATA[33]	IO_VB8N2_AG24	AG24	A18
CB4_DATA[34]	IO_VB8N2_AG25	AG25	B17
CB4_DATA[35]	IO_VB8N1_AG26	AG26	B18
CB4_DATA[36]	IO_VB8N4_AH21	AH21	A19
CB4_DATA[37]	IO_VB8N3_AH22	AH22	A20
CB4_DATA[38]	IO_VB8N3_AH23	AH23	B19
CB4_DATA[39]	IO_VB8N2_AH24	AH24	B20
CB4_DATA[40]	IO_VB8N2_AH25	AH25	A21
CB4_DATA[41]	IO_VB8N1_AH26	AH26	A22
CB4_DATA[42]	IO_VB8N1_AH27	AH27	B21
CB4_DATA[43]	IO_VB8N4_AJ22	AJ22	B22
CB4_DATA[44]	IO_VB8N3_AJ23	AJ23	A23
CB4_DATA[45]	IO_VB8N3_AJ24	AJ24	A24
CB4_DATA[46]	IO_VB8N2_AJ25	AJ25	B23
CB4_DATA[47]	IO_VB8N2_AJ26	AJ26	B24
CB4_DATA[48]	IO_VB8N1_AJ27	AJ27	A25
CB4_DATA[49]	IO_VB8N0_AJ28	AJ28	A26
CB4_DATA[50]	IO_VB8N3_AK23	AK23	B25
CB4_DATA[51]	IO_VB8N3_AK24	AK24	B26
CB4_DATA[52]	IO_VB8N2_AK25	AK25	A27
CB4_DATA[53]	IO_VB8N2_AK26	AK26	A28
CB4_DATA[54]	IO_VB8N1_AK27	AK27	B27
CB4_DATA[55]	IO_VB8N0_AK28	AK28	B28
CB4_DATA[56]	IO_VB8N4_AL22	AL22	A29
CB4_DATA[57]	IO_VB8N3_AL23	AL23	A30
CB4_DATA[58]	IO_VB8N3_AL24	AL24	B29
CB4_DATA[59]	IO_VB8N2_AL25	AL25	B30
CB4_DATA[60]	IO_VB8N2_AL26	AL26	A31
CB4_DATA[61]	IO_VB8N1_AL27	AL27	A32
CB4_DATA[62]	IO_VB8N0_AL28	AL28	B31
CB4_DATA[63]	IO_VB8N4_AM21	AM21	B32

CB4_DATA[64]	IO_VB8N4_AM22	AM22	B34
CB4_DATA[65]	IO_VB8N3_AM23	AM23	B49
CB4_DATA[66]	IO_VB8N3_AM24	AM24	B50
CB4_DATA[67]	IO_VB8N2_AM25	AM25	B51
CB4_DATA[68]	IO_VB8N2_AM26	AM26	B52
CB4_DATA[69]	IO_VB8N1_AM27	AM27	A53
CB4_DATA[70]	IO_VB8N0_AM28	AM28	A54
CB4_DATA[71]	IO_VB8N0_AM29	AM29	B53
CB4_DATA[72]	IO_VB8N4_AN22	AN22	B54
CB4_DATA[73]	IO_VB8N3_AN23	AN23	A55
CB4_DATA[74]	IO_VB8N3_AN24	AN24	A56
CB4_DATA[75]	IO_VB8N2_AN25	AN25	B55
CB4_DATA[76]	IO_VB8N2_AN26	AN26	B56
CB4_DATA[77]	IO_VB8N1_AN27	AN27	A57
CB4_DATA[78]	IO_VB8N0_AN28	AN28	A58
CB4_DATA[79]	IO_VB8N0_AN29	AN29	B57
CB4_DATA[80]	IO_VB8N4_AP20	AP20	B58
CB4_DATA[81]	IO_VB8N4_AP22	AP22	A59
CB4_DATA[82]	IO_VB8N3_AP23	AP23	A60
CB4_DATA[83]	IO_VB8N3_AP24	AP24	B59
CB4_DATA[84]	IO_VB8N1_AP26	AP26	B60
CB4_DATA[85]	IO_VB8N1_AP27	AP27	A61
CB4_DATA[86]	IO_VB8N0_AP29	AP29	A62
CB4_DATA[87]	IO_VB8N2_AR24	AR24	B61
CB4_DATA[88]	IO_VB8N2_AR25	AR25	B62
CB4_DATA[89]	IO_VB8N1_AR26	AR26	A63
CB4_DATA[90]	IO_VB8N1_AR27	AR27	A64
CB4_DATA[91]	IO_VB8N0_AR28	AR28	B63
CB4_DATA[92]	IO_VB8N0_AR29	AR29	B64
CB4_DATA[93]	IO_VB8N4_AT24	AT24	A65
CB4_DATA[94]	IO_VB8N3_AT25	AT25	A66
CB4_DATA[95]	IO_VB8N3_AT26	AT26	B65
CB4_DATA[96]	IO_VB8N3_AT27	AT27	B66

Table 8.21: Pin connection to the module connector: *Hpe_childboard* 4 connector.

The differential signals *CB4_CLK** are connected to PLL output pins of the PLL 11.

8.8.3 Power Reset

The signal *PWR_RESET#* table 8.22 is the global reset signal for the whole system. It is delivered via the module connector. This reset is low active, activated after power up and controlled by a supervisor on the *Hpe_midi*.

Signal Name	*FPGA Pin Name*	*FPGA Pin Number*
PWR_RESET#	DEV_CLRn	AN21

Table 8.22: Pin connection to the module connector: Global Reset.

9 Specifications

Model:	*HMX2-AS2-180*

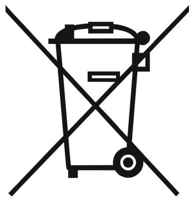
9.1 HMX2-AS2 Board

Mechanical	
Dimensions:	226 mm [W] * 226 mm [D]
Net weight:	x kg
Environmental Considerations:	0 – 50 °C

9.1.1 HMX2-AS2 in the case

Mechanical	
Dimensions:	325 mm [W] * 265 mm [D] * 75 mm [H]
Net weight:	1,85 kg
Environmental Considerations:	0 – 50 °C
Ingress protection:	IP40 to EN60529
Surface treatment:	powder coating
Enclosure body Material|Color:	Al Si 12|RAL 9005, black
Foot elements Material|Color:	ABS|RAL 3003, ruby red

9.2 WEEE



Based on the Ordinance on Waste Prevention, Collection and Treatment of Waste Electrical and Electronic Equipment (WEEE Ordinance) we offer all European customers to send back their Hpe equipment at end of life. We will take care of the correct waste management. Our GLN Nr. is 900 83 90 46 78 48

Index