



Industrial Reference Platform

The Industrial Reference Platform is designed to help developers create powerful and efficient solutions that meet custom or application-specific requirements. The system consists of four interdependent components:

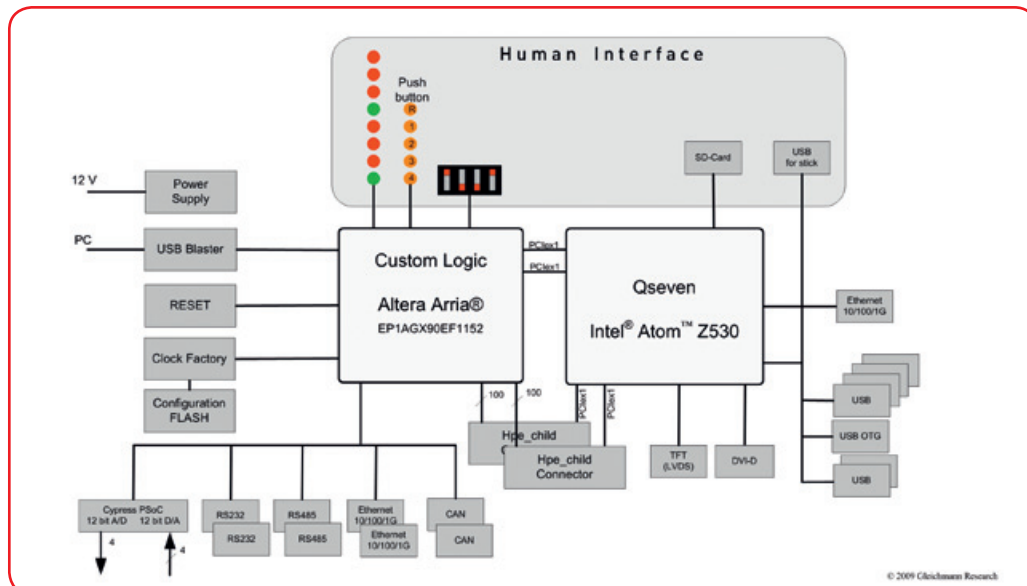
- **Hpe®_IRP** – Modular system in an enclosure including complete tool chain
- **MSC Qseven™ Module** – Intel® Atom™ Processor Z530 (@1,6GHz)
- **Altera® Arria® FPGA** – Programmable logic flexibility with high-speed transceivers
- **Software package** – Real-time LINUX and preinstalled 3S CoDeSys

Hpe[®] IRP Industrial Reference Platform

1. Introduction

Gleichmann Electronics Research announces a new **Industrial Reference Platform**. The heart of this platform is an Intel[®] Atom[™] processor and an Altera[®] Arria[®] FPGA, connected with PCI Express (PCIe) to support customer-specific interface and logic requirements. The system is based on the GE-Research Hpe[®] (Hardware prototype and emulation) platform, an expandable base board with a range of different interfaces in a durable enclosure – ideal for software developers. The base board carries a MSC Qseven[™] module with the CPU system, two child board connectors for custom logic implementations and a set of peripheral interfaces. For system prototyping and hardware developers, the enclosure can be opened to allow easy and rapid access to the expansion ports.

2. Hpe[®]_IRP System Overview



The block diagram of the Hpe[®]_IRP shows all components and interfaces of the development platform. The boxes below list these components:

Components Controlled by Intel Atom

- 250-GB SATA2 hard disk
- DVI-D and LVDS for display
- 1-Gb Ethernet for CPU control
- 1 USB in the front panel (for stick)
- 1 SD-Card in the front panel
- 3 USBs in the rear panel
- 4 USBs on an internal header

Physical Interfaces on Board

- 2 x 10/100/1G Ethernet for Fieldbus
- 2 x CAN for Fieldbus
- 2 x RS485 Ethernet for Fieldbus
- 2 x RS232
- 4 x 12-bit A/D and D/A (Cypress PSoC)
- 8 optical IN and optical OUT

System Components

- ALTERA[®] USB-Blaster[™] on board
- 2 x 20-character LCD display
- 8 LEDs
- 5 push-buttons
- 1 DIP switch
- 2 connectors for Hpe[®] child boards
- Programmable clock factory with 7 input clocks
- GE-Research SEulator connector for higher quality system development

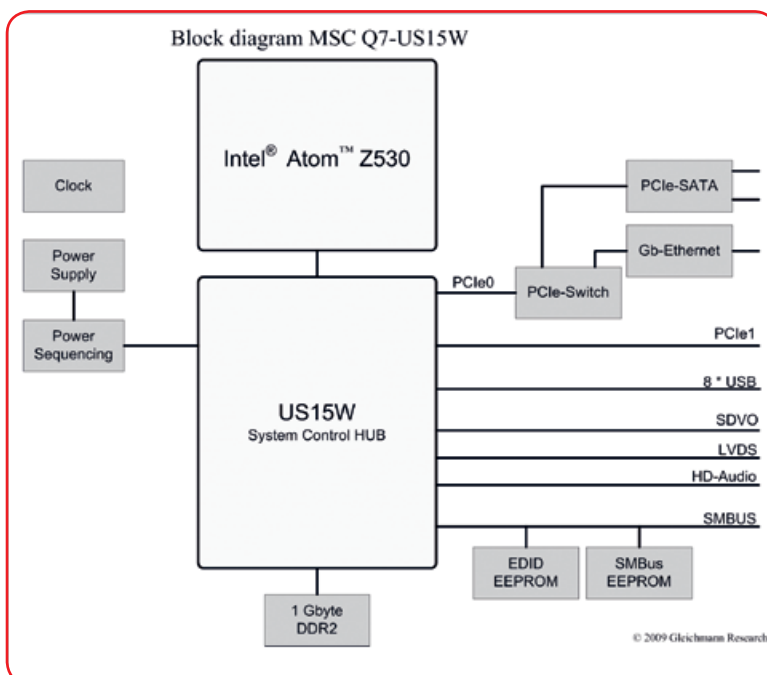
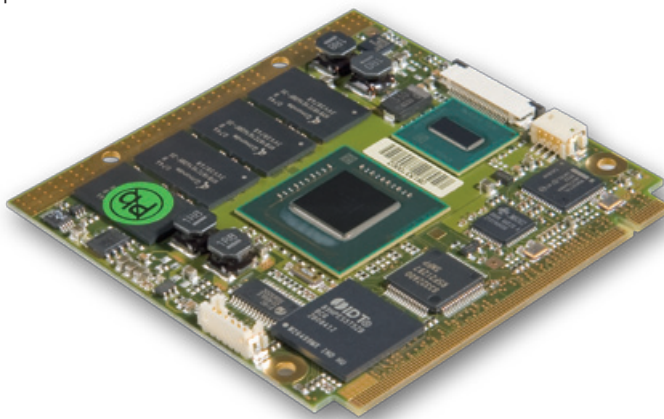
3. MSC Qseven™ Module



The Qseven™ concept is an off-the-shelf, multi-vendor, single-board-computer that integrates all the core components of a common PC and is mounted onto an application-specific carrier board. Qseven™ modules have a standardized 70-mm x 70-mm form factor and specified pin outs based on the high-speed MXM system connector, which has standardized pin outs regardless of the vendor. The Qseven™ module provides the functional requirements for an embedded application. These functions include, but are not limited to, graphics, sound, mass storage, network and multiple USB ports. A single ruggedized MXM connector provides the carrier board interface to carry all the I/O signals to and from the Qseven™ module.

More information on www.qseven-standard.org

- Intel® Atom™ Processor Z530, 1,6GHz low power CPU
- 1-GB DDR2 SDRAM on board
- 2 SATA-300 mass storage Interfaces
- 10/100/1000 Base-TX Ethernet interface
- LVDS interface (18-/ 24-bit) up to 1600 x 1200
- 3 PCIe x1 lanes
- 8 USB 2.0 interfaces
- Cost-effective standardized embedded PC module for industrial solutions



4. Altera® Arria® FPGA for customization

The Arria® FPGA connects directly to the Intel® Atom processor via PCIe to offer a high-speed connection to the flexibility offered by the programmable logic. By using the FPGA, it is possible to prototype and test a wide range of applications to leverage the available IP and system-debug features of the Hpe®_IRP.

Key features of the Altera® Arria® FPGA implementation include:

- Numerous on-board interfaces
- High-speed PCIe CPU to FPGA link
- Easy-to-use system design tool including professional IP library
- Complete GE-Research FPGA debugging tool support
- SEmulator® link for higher design quality
- On-board Altera® USB Blaster and clock factory
- Design services and support from GE-Research

5. Development support

The Hpe®_IRP system (based on the Hpe®_midi system) includes a complete set of tools to help the developer achieve a seamless hardware and software development flow. Supplying the best software tools ensures the maximum potential can be realized from excellent hardware in minimum time. The GE-Research Hpe® tools guarantee this close collaboration between hardware and software.

By delivering a complete set of high-quality tools that are tailored and optimized to work with this development platform.

5.1 Hpe®_desk

The Hpe®_desk is a graphical development environment that contains these tools:



- Clock factory
- Hpe® JTAG
- Hpe®_AIM
- IP Evaluation Package
- SEmulator® with associated functions (not included in the free package)

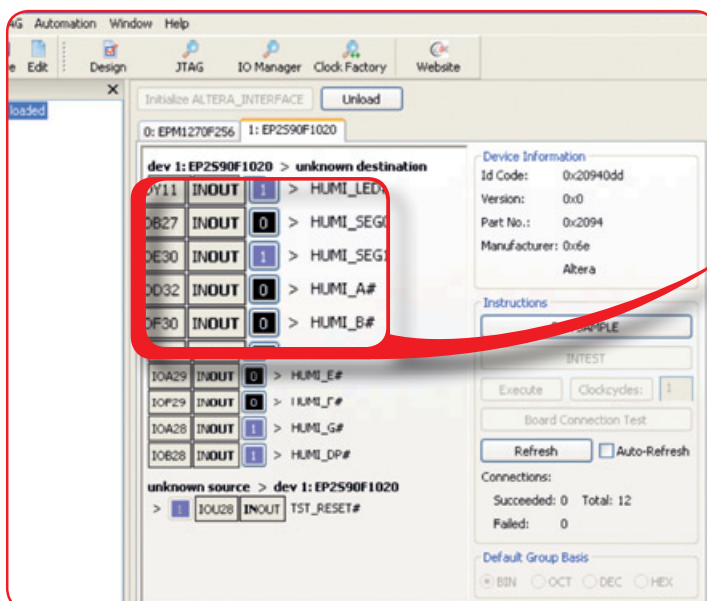
5.2 Clock factory



The Hpe[®]_IRP supports several clock sources: one system clock (crystal based), two PLL outputs (from FPGA) and one external clock via SMA connector. These clocks can be routed by a CPLD to any of the 7 clock inputs of the FPGA. The developer needs no special knowledge of the hardware as this routing can be easily controlled using the clock factory tool. This tool allows the configuration and management of the CPLD and clocks to be managed entirely from the graphical user interface shown below:

5.3 Hpe[®]_JTAG

Hpe[®]_JTAG is a boundary scan tool for interactive PCB debugging that provides a graphical user interface with powerful Python scripting capabilities. The screenshot below shows an example of a scan chain containing two JTAG compatible devices (each represented by a tab). In the context of the Hpe_IRP system it can be used for non intrusive signal observation of any hardware interface that is accessible with boundary scan. For instance users can step through their embedded code and observe the effects on the hardware even for interfaces that are not accessible on the board.



I/O-Filtering:

Instead of showing the whole grid array (each with over a thousand I/Os) a filter function allows the user to display only I/Os that are currently of interest.

Pin-File Parsing:

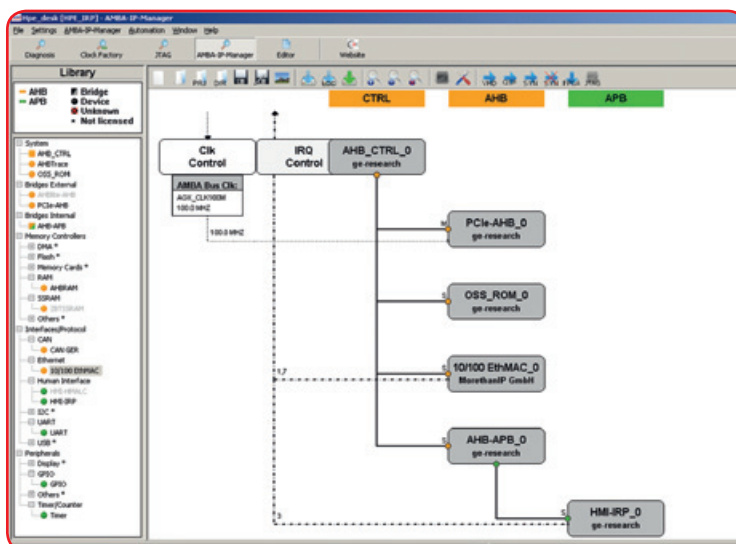
Use the HDL top-level pin names to find signals.

5.4 Hpe®_AIM (Advanced IP Manager)

The system is delivered with a library with intellectual property (IP) from a range of IP providers. These IP blocks offer a modular set of functions that enables the user to quickly and easily build a fully integrated custom system using the Hpe®_AIM tool. GE-Research only adds certified macros to this library, which must meet these requirements:

- Availability of a demonstration design, which developers can use for reference
- Functional check of IP in standard configurations
- Availability of test pattern
- Datasheet and description

The working window of the Hpe®_AIM consists of five different panes. Key areas of interest are the top right and middle panes (see picture below). The middle pane shows all currently installed macros, from which the developer can drag and drop any available IP component to the top right window, where it is automatically connected to the bus system. The developer then can modify the generic parameters of the component by right-clicking the block. If the IP is only available as netlist, only the AHB address and mask are configurable. Contextual tooltips give instant information about the characteristics of each of the IP blocks (e.g., vendor, price, size).



The Hpe®_AIM offers a complete design flow from IP design all the way through to programming into the FPGA.

Generate a complex FPGA with only 4 Mouse Clicks!

5.5 GE-Research Basic Package

For free evaluation and really low license cost our customers will get a set of

- BUS Arbiter with multi master support
- DMA Controller
- Clock and Interrupt Controller
- PCI Express to AHB bridge (MSI and MSIx support)
- Internal AHB to APB bridge
- OSS-ROM (Operating System Support ROM)
- RAM, ROM, FIFO generator
- Generator for customer specific IP
- UART, I2C, CAN2.0b
- Ethernet 10/100 ,GPIO, Timer, Counter, PWM

... and last but not least complete LINUX OSADL support

5.6 SEmulator®

The SEmulator tool helps the developer **increase the speed and quality of the design process**. The hardware offers a high speed link of 2.5 Gbps between the PC and the Arria® FPGA. The SEmulator is connected directly via PCI Express to the host PC. Highlights of the SEmulator include:

- **Hardware Acceleration:** The FPGA can be used as accelerator for Mentor ModelSim or ALDEC ActiveHDL simulator. Simulation speed-up of up to 600 times is possible: (10 hour simulation time drops to 1 minute!)
- **Hardware in the Loop:** Every real hardware component on the module, base board or any child board can be used as an actual and absolutely correct simulation model.
- **Logic Analyzer:** Based on Altera's signal tap, but use data storage on the PC rather than the FPGA for superior storage capacity.
- **Hardware Fault Injector:** STUCK@, pulse, multiple pulses, SEU and MEU are combined with the acceleration and benefits of analysis software.

These tools have been designed to increase the quality of a design and decrease development time! For more detailed information on these tools, please see www.ge-research.com.

6. Features and Specifications

Intel® Atom™ Z530 Processor	Altera® Arria® GX Series FPGA
1.6-GHz processor frequency	TriMatrix memory structure performance up to 380 MHz
IA32 architecture	12 transceiver channels (600 Mbps to 3.125 Gbps)
32-KB instruction and 24-KB data (L1) caches	Optional Nios® II embedded processor
512-MB, 8-way set-associative L2 cache	Multiple clock networks, RAM blocks, and digital signal processing (DSP) blocks
533-MHz Front-Side Bus (FSB)	90,220 logic elements for system design
2.2-W maximum TDP (power)	Up to 538 I/O pins
13-mm x 14-mm package, PBGA 441 Socket	35-mm x 35-mm 1,152-pin FBGA package
System Features	
Intel® SCH US15W chipset with I/O controller on Qseven™ board (4.5 W)	2 x 20 characters LCD display and 8 LEDs for information display and system debug
1-GB DDR system memory	Factor clock and reset control
3x Gigabit Ethernet ports (1 PCIe module on Qseven™, 2 ports on the FPGA board)	8-input/8-output opto-isolated I/Os, 16 GPIOs, 5 push-buttons, and 4 DIP switches
2x SATA-2 controllers (PCIe) module	2x CAN interfaces
250-GB HDD pre-installed with Linux OSADL	2x RS-485 fieldbus interfaces
DVI-D interface or internal LVDS backlit kit	2x RS-232 serial interfaces
8 USB 2.0 ports	4x A/D and 4x D/A converters
SD card socket	Configuration FLASH
PCIe x1 interface to the FPGA	Altera® USB-Blaster™
291-mm x 74-mm x 100-mm (L x W x H)	110/230VAC PSU (12V VDC input)
MSC Hpe®_desk development/debug tools, including JTAG and SEmulator®	Altera® Quartus® II design software with SOPC Builder (download)
Software Package	
Linux OSADL	
3S CoDeSys IEC61131 run-time software (evaluation copy)	
Reference design examples	
Pre-installed reference platform configuration	

About Gleichmann Research



Softwarepark Hagenberg

Gleichmann Electronics Research (GE-Research) was founded in October 2004 in Hagenberg, Austria with the goal to turn research prototypes into products. Having unconventional ideas, developing new, creative solutions as well as new and innovative products in close cooperation with universities and industrial partners is our daily challenge.

In close cooperation with the University of Hagenberg and other universities, GE-Research develops FPGA and ASIC design tools as well as system-on-chip (SoC) solutions. The first hardware accelerator and co-simulator prototype was developed by Prof. Dr.-Ing. Markus Pfaff back in 1999. Since then, it has been a long and stony way to shipping the first hardware accelerator and co-simulator HAC1 in 2005 and, soon after, the HAC2 in 2006. At the same time, GE-Research successfully established its hardware prototyping and emulation systems, Hpe[®], on the market. The SEmulator[®] combines these two product lines and turns them into one. Unlike expensive high-end hardware accelerators, the SEmulator[®] is based on emulation hardware, such as the configurable and customizable Hpe[®]_midi FPGA/ASIC prototyping system, and is extended with a fast PCIe link to the host PC. SEmulator[®], a synthetic word that combines the words simulation and emulation, describes the basic functionality of the SEmulator[®] very well: the SEmulator[®] provides bridging functionality between the domain of digital hardware simulation and the world of FPGA/ASIC prototyping.



FH Hagenberg



Softwarepark Hagenberg

Together with the Gleichmann Electronics design centre in Eching, we employ more than 10 highly qualified engineers with many years experience in the field of FPGA and ASIC design. In 2007, GE-Research relocated to new facilities allowing aggressive growth for the years to come. GE-Research has formed many partnerships with companies to complement its know-how for complex and future-oriented solutions.



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